ICG-1020S

Miniature Dual-Axis OIS-Optimized MEMS Gyroscope

GENERAL DESCRIPTION

The ICG-1020S dual-axis MEMS angular rate sensor is designed for optical image stabilization (OIS) applications in smartphone camera modules and other mobile devices.

The ICG-1020S supports up to 32 kHz ODR for backward compatibility to other InvenSense dedicated OIS gyroscope products. This device provides extremely low RMS noise as well as noise density.

The high-resolution gyros support a programmable full-scale range of ±46.5 dps to ±374 degrees/sec, fast sample rate at up to 32 KHz, low phase delay including a fast 20 MHz SPI interface, very low rate noise at 4 mdps/√Hz, and extremely low power consumption at 2.5 mA. Precise sensitivity control allows a calibration-less strategy for gyroscope to save production cost and time by eliminating the shake table.

ORDERING INFORMATION

PART	AXES	TEMP RANGE	PACKAGE
ICG-1020S	X,Y	-40°C to +85°C	12-Pin LGA

†Denotes RoHS and Green-Compliant Package

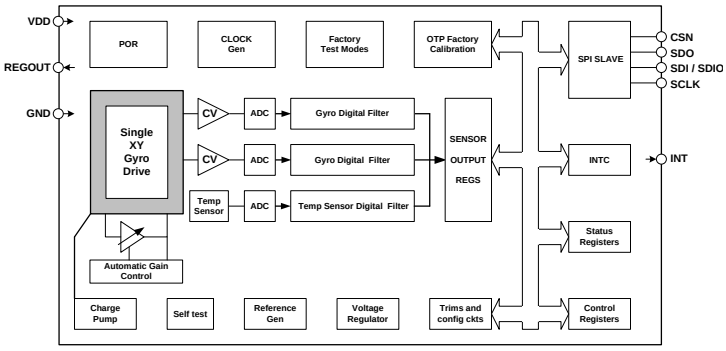
APPLICATIONS

- Smart Phone Camera Modules
- Digital Still Camera and Video Cameras
- High Resolution / Low Noise Applications

FEATURES

- Small 2.3 x 2.3 x 0.65 mm LGA Package
- Very Low 4 mdps/√Hz Rate Noise
- Extremely tight sensitivity eliminates OIS dynamic calibration
- LPF with 40, 80, 160, 250 and 500 Hz settings
- Programmable high-pass filters at 0.05 to 10 Hz to remove offset drift due to temperature & PCB warp
- Independent ODR v. LPF selection for the most optimized performance
- Narrow FSR Range from ±46.5 dps to ±374 dps
- High Resolution at up to 700 LSB/(º/s)
- Fast Start Up Time; Sleep to Ready at 35 ms
- SPI (3 & 4 Wire) Interface
- Fast 20 MHz SPI Interface
- Temperature sensor for offset temp compensation
- Wide 1.7 V to 3.6 V Supply Voltage Range
- Low 5 mW Active Power & 6µA Sleep Mode
- Self-test allows quick gyro functionally check
- High 10,000*g* Shock Survivability

BLOCK DIAGRAM



TYPICAL OPERATING CIRCUIT

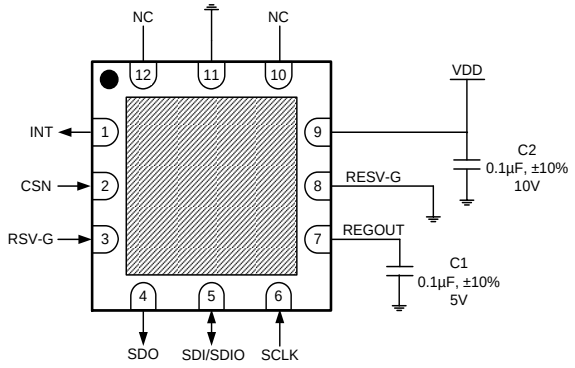


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TABLE OF CONTENTS

1. INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design-related information on the ICG-1020S MotionTracking device. The device is housed in a small 2.3 x 2.3 x 0.65 mm LGA Package.

1.2 PRODUCT OVERVIEW

The ICG-1020S is digital output, 2 Axis MEMS gyroscope IC optimized for Optical Image Stabilization applications in mobile devices such as Smartphones, Tablets and Digital Still Cameras. The single structure vibratory MEMS rate gyroscope detects rotation about the X and Y axis. When the gyro is rotated about any of the sense axes, the Coriolis effect causes a vibration that is detected. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate.

This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The FSR range is optimized for image stabilization applications where the narrower range improves hand jitter detection accuracy. User-selectable low-pass filters enable a wide range of cut-off frequencies.

The ICG-1020S uses fixed clocking scheme that results in a fixed ODR up to 32 kHz for the host to sample the raw gyro output. The combination of multiple options for DLPF cut-off frequency (40/160, 80/320, 160/640, 250, and 500 Hz) and very low noise provides the best performance in OIS applications where high bandwidth and low noise provide fast and stable servo loop, resulting in extended exposure times with lower possibility of blur

1.3 APPLICATIONS

- Smart Phone Camera Modules
- Digital Still Camera and Video Cameras
- High Resolution / Low Noise Applications

2. FEATURES

- Small 2.3 x 2.3 x 0.65 mm LGA Package
- Very Low 4 mdps/√Hz Rate Noise
- Extremely tight sensitivity eliminates OIS dynamic calibration
- LPF with 40, 80, 160, 250 and 500 Hz settings
- Programmable high-pass filters at 0.05 to 10 Hz to remove offset drift due to temperature & PCB warp
- Independent ODR v. LPF selection for the most optimized performance
- Narrow FSR Range from ±46.5 dps to ±374 dps
- High Resolution at up to 700 LSB/(º/s)
- Fast Start Up Time; Sleep to Ready at 35 ms
- SPI (3 & 4 Wire) Interface
- Fast 20 MHz SPI Interface
- Temperature sensor for offset temp compensation
- Wide 1.7 V to 3.6 V Supply Voltage Range
- Low 5 mW Active Power & 6µA Sleep Mode
- Self-test allows quick gyro functionally check
- High 10,000*g* Shock Survivability

3. ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, VDD = 2.5 V and T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
Sensor Specifications						
GYRO SENSITIVITY						
Full-Scale Range	FS_SEL = 0 (default) FS_SEL = 1 FS_SE L =2 FS_SEL = 3		±46.5 ±93 ±187 ±374		º/s º/s º/s º/s	1
Sensitivity Scale Factor	FS_SEL = 0 FS_SEL = 1 FS_SEL = 2 FS_SEL = 3		700 350 175 87.5		LSB/(º/s) LSB/(º/s) LSB/(º/s) LSB/(º/s)	1
Gyro ADC Word Length			16		bits	
Sensitivity Scale Factor Tolerance	+25°C		±1		%	1
Sensitivity Scale Factor Variation Over Temperature	-20°C to +75°C		±2		%	2
Nonlinearity	Best fit straight line; 25°C		±0.1		%	2
Cross-Axis Sensitivity	Manufacturing Tolerance Characterized PCB level		±2 ±2		% %	1 2
175GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C PCB Level		±3 ±15		º/s º/s	1 2
ZRO Variation Over Temperature	-20°C to +75°C		±3		º/s	2
GYRO NOISE PERFORMANCE	FS_SEL = 0, Fchoice_B = 0					
Total RMS Noise	DLPFCFG = 0 (3.36 kHz) DLPFCFG = 2 (40 Hz) DLPFCFG = 2 (80 Hz) DLPFCFG = 2 (160 Hz) DLPFCFG = 2 (250 Hz, default) DLPFCFG = 2 (500 Hz)		0.85 0.03 0.04 0.06 0.07 0.09		º/s-rms º/s-rms º/s-rms º/s-rms º/s-rms º/s-rms	2 5 5 5 5 5
Group Delay	DLPFCFG = 0 (3.36 kHz) DLPFCFG = 2 (40 Hz) DLPFCFG = 2 (80 Hz) DLPFCFG = 2 (160 Hz) DLPFCFG = 2 (250 Hz) DLPFCFG = 2 (500 Hz)		0. 17 6.41 3.09 1.59 1.07 0.61		 ms 	6 6 6 6 6 6
Low-frequency RMS noise **Rate Noise Spectral Density**	Bandwidth 1 Hz to10 Hz Bandwidth 0.1 Hz to 1 Hz At 10 Hz		0.012 0.004 0.004		º/s-rms º/s-rms º/s/√Hz	1 1 1
GYRO MECHANICAL Mechanical Frequency Useful mechanical signal BW **Ultrasonic Wash Frequencies**		 25.6 36	 27 	 29 1.6 40	 kHz kHz kHz	 1 1 4
VDD POWER SUPPLY Operating Voltage Range		1.7		3.6	V	2
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	1		100	ms	2
Normal Operating Current	Two Axes Active		2.5		mA	1
Sleep Mode Current			6		µA	1
GYRO START-UP TIME ZRO Settling	DLPFCFG=0, to ±1º/s of Final From Sleep Mode to ready From Power On to ready		 25 35		 ms ms	 1
OPERATING TEMPERATURE RANGE		-40		+85	ºC	2
DIGITAL INPUTS (AD0, SCLK, SDI, $\overline{CS}$) VIH, High Level Input Voltage		 0.7*VDD -0.5		 VDD+0.5 0.3*VDD	 V V	2

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
VIL, Low Level Input Voltage CI, Input Capacitance			< 5		pF	
DIGITAL OUTPUT (INT, SDO) V_{OH}, High Level Output Voltage V_{OL1}, LOW-Level Output Voltage $V_{OL.INT1}$, INT Low-Level Output Voltage		0.9*VDD		0.1*VDD 0.1	 V V V	2
V_{hys}, Hysteresis			0.1*VDD		V	2
V_{OL1}, LOW-Level Output Voltage	3 mA sink current		0 to 0.4		V	2
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4 V V_{OL} = 0.6 V		3 6		mA mA	2
Output Leakage Current			100		nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf		20+0.1C_b to 250		ns	2
C_i, Capacitance for Each I/O pin			< 10		pF	2
INTERNAL CLOCK SOURCE						2
Sample Rate	Fchoice_B = 0 and SMPLRT_DIV ≥ 0		8		kHz	1
	Fchoice_B = 1 and SMPLRT_DIV ≥ 1					2
	Fchoice_B = 1 and SMPLRT_DIV = 0		32			2
Clock Frequency Initial tolerance	CLK_SEL = 0, 6; 25°C	-5		+5	%	2
	CLK_SEL = 1,2,3,4,5; 25°C	-1		+1	%	2
Frequency Variation over Temperature	CLK_SEL = 0,6		-10 to +10		%	2
	CLK_SEL = 1,2,3,4,5		±1		%	2

Notes:
1. Tested in production
2. Derived from validation of characterization of parts, not guaranteed in production
3. Assumes environmental noise less than 2dps
4. Please refer to Ultrasonic Wash Application Note
5. Calculated based on specified rate noise
6. Guaranteed by design. Corner frequency is specified for each individual DLPF filter (-3dB for DLPFCFG = 2 and -6dB for DLPFCFG = 3)

3.1 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5 V to 4.0 V
REGOUT	-0.5 V to 2 V
CSN, SCLK, SDI/SDIO, SDO	-0.5 V to VDD
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2 ms
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 250 V (MM)
Latch-Up	JEDEC Class II (2),125°C, ±100 mA

4. TIMING CHARACTERISTICS

4.1 SPI TIMING DIAGRAMS (4- WIRE AND 3-WIRE)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
A	$t_{SU.CS}$ CS Setup Time		13	-	-	ns	1
B	$t_{SU.SDI}$ SDI Setup Time		5	-	-	ns	1
C	$t_{HD.SDI}$ SDI Hold Time		7.5	-	-	ns	1
D	$t_{VD.SDO}$ DO Valid Time	C_{load} = 20pF	-	-	30	ns	1
E	f_{SCLK} SCLK Clock Frequency		-	-	20	MHz	1
F	t_{HIGH} SCLK High Period		24	-	-	ns	1
G	t_{LOW} SCLK Low Period		24	-	-	ns	1
H	$t_{HD.SDO}$ SDO Hold Time		4	-	-	ns	1
I	$t_{HD.CS}$ CS Hold Time		25	-	-	ns	1
J	$t_{DIS.SDO}$ SDO Output Disable Time		-	-	32	ns	1
-	t_{BUF} CS high time between transactions		400	-	-	ns	1

Note 1: Derived from validation or characterization of parts, not guaranteed in production.

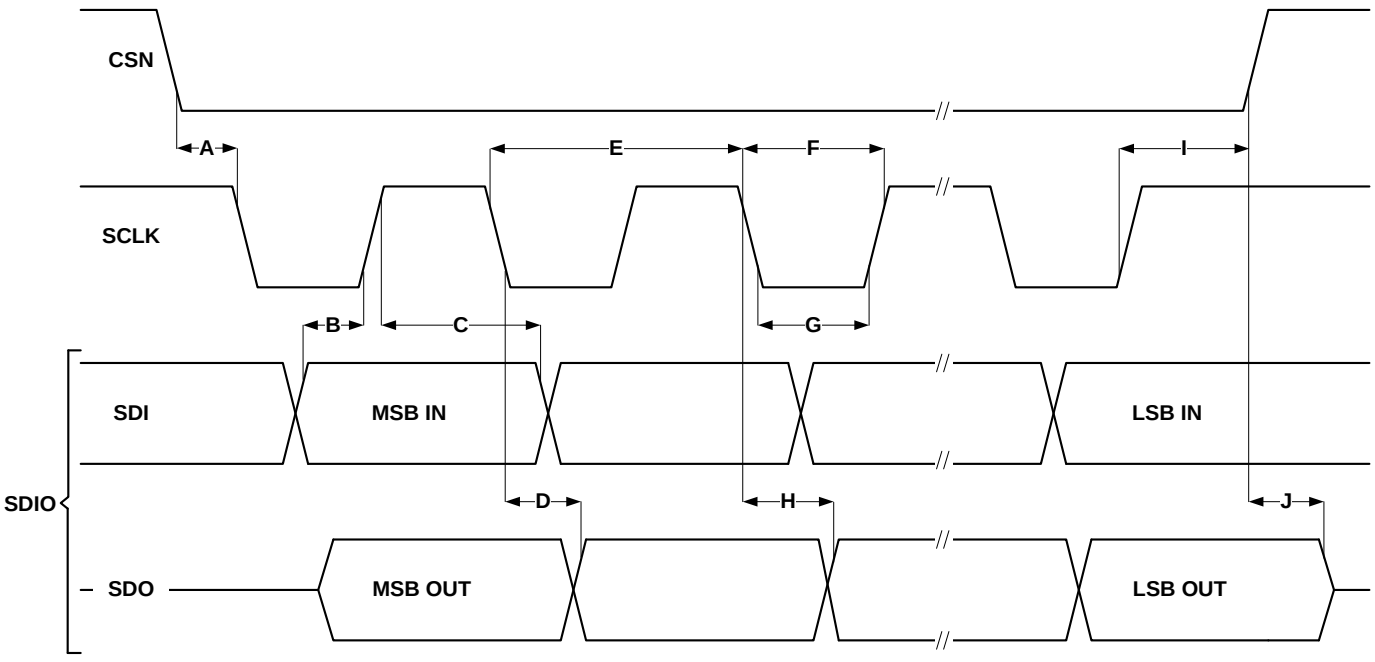


Figure 1a. SPI Timing Diagrams for 4- and 3-Wire CPOL = 1

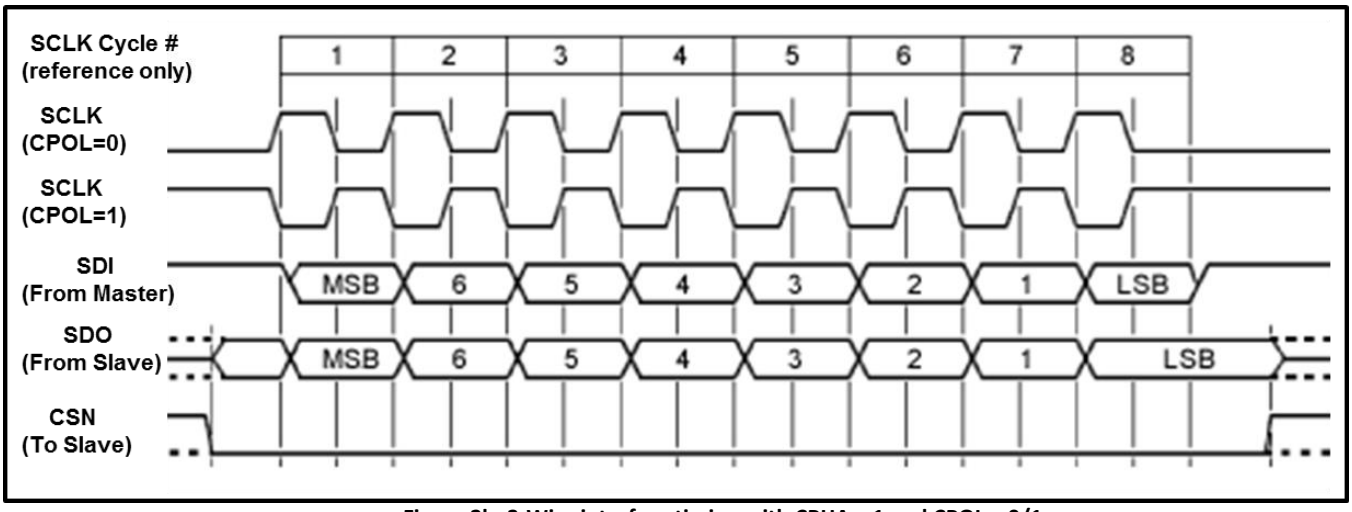


Figure 2b. 3-Wire interface timing with CPHA = 1 and CPOL = 0/1
3-wire Interface Clocks Data into the Slave on the Clock's Rising Edge and Data Out of the Slave on the Clock's Falling Edge

For 3-wire SDI will operate as SDIO and will go to high Z when CSN is at logic 1. SDIO will obey SDI timing when operating as input and SDO timing when operating as output.

5. APPLICATION INFORMATION

5.1 PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	INT	Interrupt Output (Totem Pole or Open-Drain)
2	CSN	SPI Chip Select Input
3	RSV-G	Reserved Pin, Connect to GND
4	SDO	SPI Serial Data Output 4-wire SPI / Float During Power-Up 3-wire SPI
5	SDI / SDIO	SPI Serial Data Input in 4-wire SPI / Serial Data In Out In 3-wire SPI
6	SCLK	SPI Serial Clock Input
7	REGOUT	On-Chip Regulator Output. Connect to GND through a 0.1 µF Capacitor
8	RSV-G	Reserved Pin. Connect to GND
9	VDD	Power Supply. Bypass to GND with a 0.1 µF Cap
10,12	RSV-N	Reserved Pin. No Connect
11	GND	Power Supply Ground

5.2 PIN CONFIGURATION

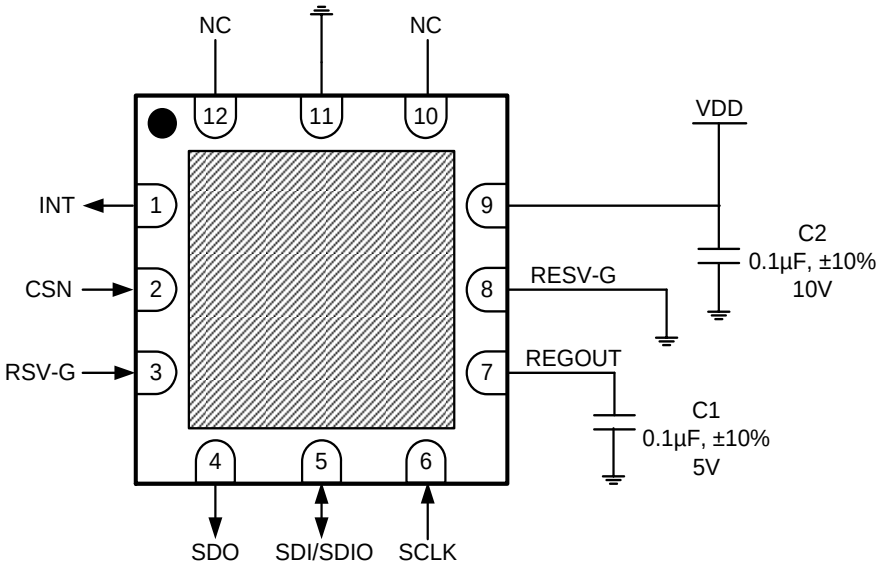


Figure 2. Package: LGA 2.3 x 2.3 x 0.65 mm, Top View

5.3 TYPICAL OPERATING CIRCUIT

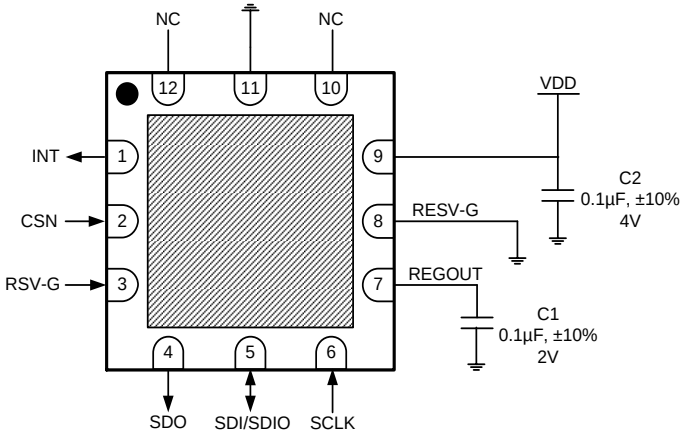


Figure 8. ICG-1020S typical application diagram (4-wire SPI bus)

5.3 BLOCK DIAGRAM

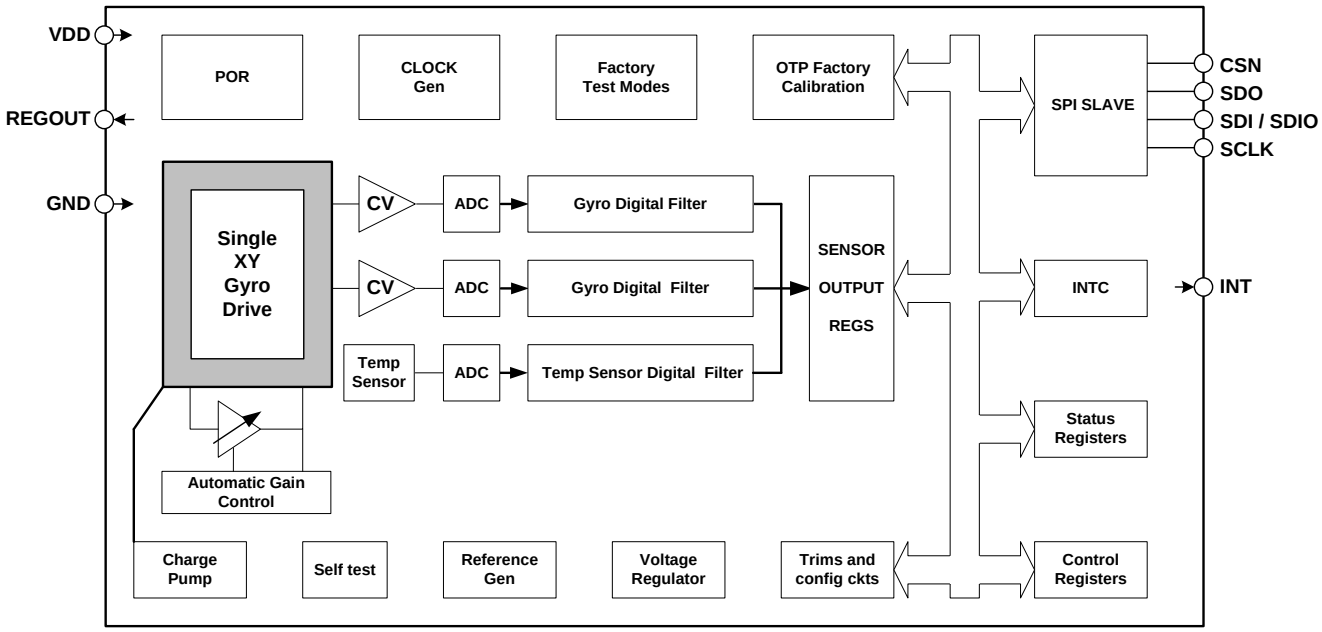


Figure 4. Block Diagram

Figure 4 identifies the key blocks. Two-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning with two axis XY configuration. After the signal is digitized, data is processed through a digital filter and output through sensor data registers. The device communicates via a register-selectable SPI serial interface. SPI provides both 4 and 3 wire options for compatibility to OIS controllers. Other blocks include on-board clocking, temperature compensation and bias circuits.

The sensor data registers contain the latest gyro data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime.

The reference generator and voltage regulator section generate the internal supply and the reference voltages and currents required by the ICG-1020S with its input as unregulated VDD of 1.7 V to 3.6 V. The voltage regulator output is bypassed by a 0.1 µF capacitor at REGOUT pin.

5.5 SYSTEM BUS LOGIC LEVELS

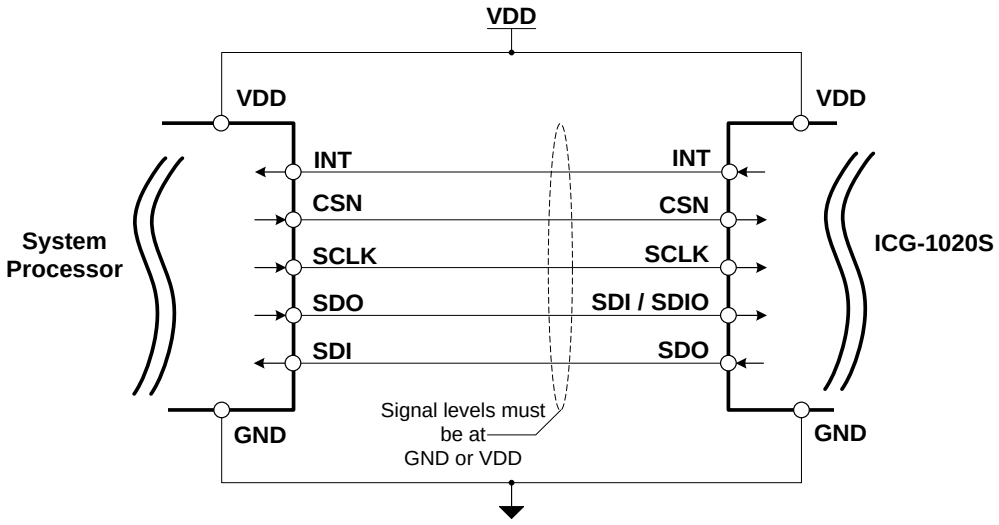


Figure 9. System Bus Logic Levels

As shown in Figure 8, the recommended logic levels for signal and data lines are 0 V and VDD.

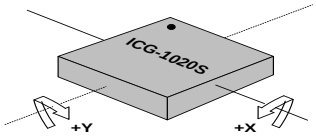


Figure 3. Orientation of Axes of Sensitivity and Polarity of Rotation
Axis Orientation and Rotation Polarity
Note the Pin 1 Identifier for ICG-1020S

5.6 DIGITAL FILTER SETTING AND PERFORMANCE

Filter choices in ICG-1020S product has been created to allow the user the flexibility of choice in tradeoffs between noise and latency. The filter structure consists of the base decimation filters, designed to clean-up ADC noise as well as to band-limit device noise; followed by the high-pass filters, which can be used to reduce offset drift, regardless of its origin; followed by a choice of 2nd order bi-quadratic filter with 5 fixed corner frequency settings (40/160, 80/320, 160/640, 250, and 500 Hz). This is illustrated in figure 5.

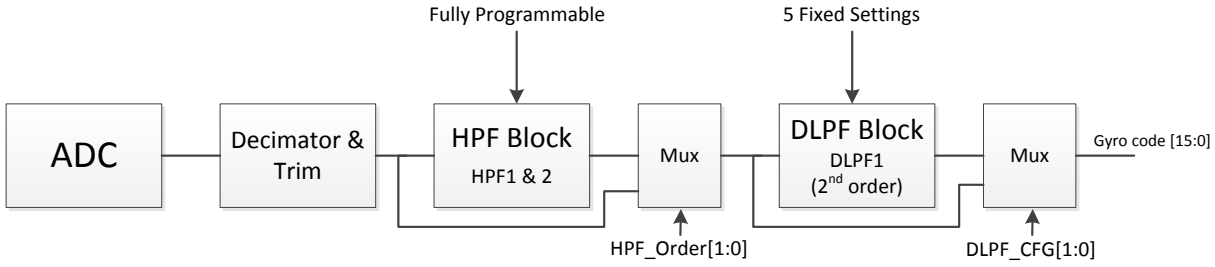


Figure 5. ICG-1020S Digital Signal Path

More detailed information about how to set these filters will be given in register map section.

6. DIGITAL INTERFACE

6.1 SPI INTERFACE

The Serial Peripheral Interface Bus (SPI) provides both 4- and 3-wire modes. The 4-wire SPI uses two control and two data lines. The ICG-1020S always operates as a Slave device during SPI operation. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDO) and the Data Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (CSN) for each Slave device; CSN goes low at the start of transmission and goes back high at the end. The SDO line remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

The 3-wire SPI uses two control and one data lines. The ICG-1020S always operates as a Slave device during SPI operation. With respect to the Master, the Serial Clock output (SCLK), and the Data Input/Output (SDIO) are shared among the Slave devices. The Master generates an independent Chip Select (CSN) for each Slave device; CSN goes low at the start of transmission and goes back high at the end. The SDIO line remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

SPI slave supports CPOL = CPHA = 0 and CPOL = CPHA = 1.

6.2 SPI OPERATION

1. Data is delivered MSB first and LSB last.
2. Data is latched on rising edge of SCLK.
3. Data should be transitioned on the falling edge of SCLK.
4. SCLK frequency is 20 MHz max.
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation.
   The following 7 bits contain the Register Address. For multiple-byte Read/Writes, data is two or more bytes;

SPI Address format

MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. SPI supports Single or Burst Read/Writes.

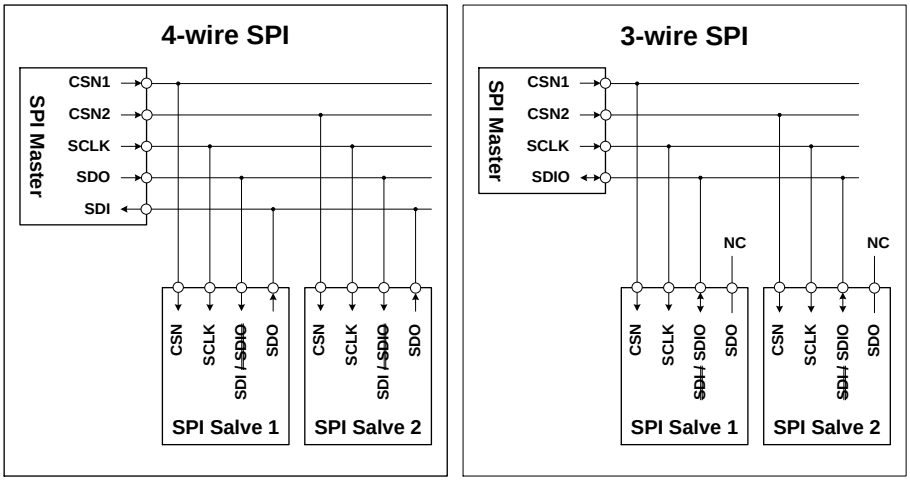
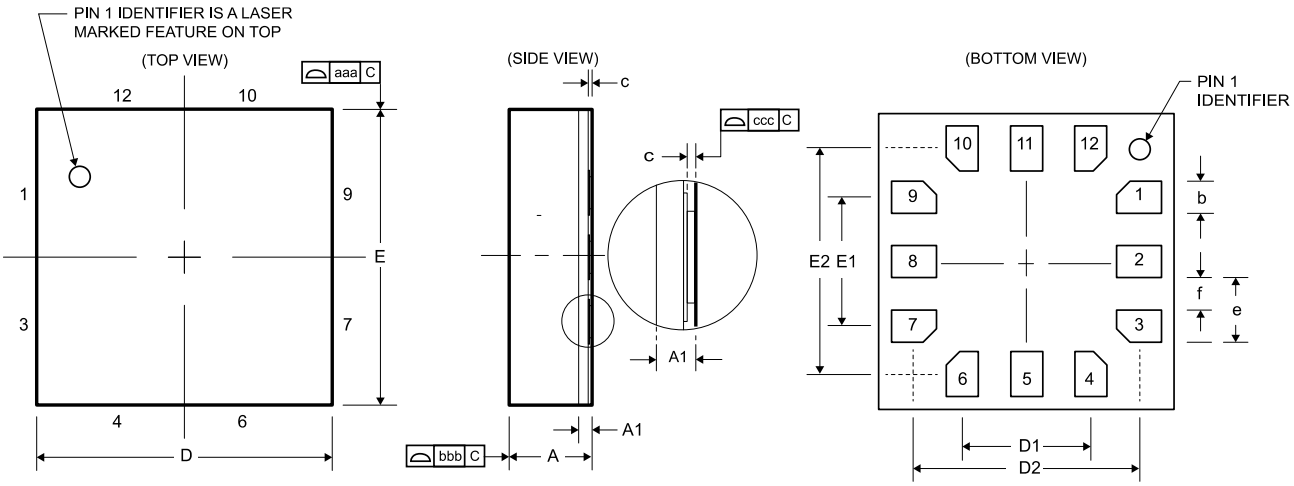


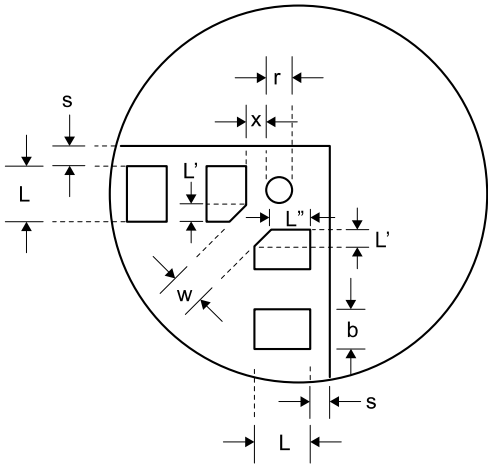
Figure 6. SPI 4-wire and 3-wire Master to Slave Connection

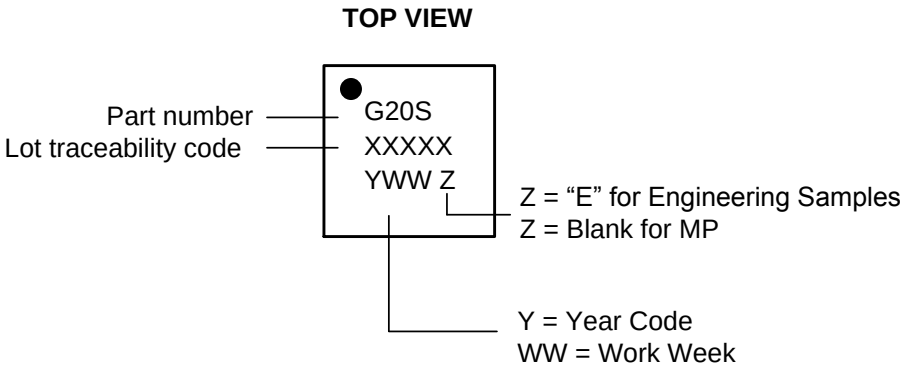
As shown in *Figure 6,* each SPI slave requires its own CSN line. SDO, SDI/SDIO and SCLK lines are shared. Only one CSN line is active (low) at a time ensuring that only one slave is selected at a time. The CSN lines of other slaves are held high which causes their respective SDO (4-wire SPI), and SDI / SDIO (3-wire SPI) pins to be high-Z.

7. PACKAGE INFORMATION



		DIMENSIONS IN MILLIMETERS		
SYMBOLS	DESCRIPTION	MIN	NOM	MAX
A	Package Thickness	0.60	0.65	0.70
A1	Substrate Thickness	---	0.105 REF	---
b	Lead Width	0.2	0.25	0.30
c	Seating Plane	---	0.08	---
D	Package Body Width	2.25	2.30	2.35
D1	Edge Lead Center to Center	---	1.00	---
D2	Center Lead Center to Center	---	1.75	---
E	Package Body Length	2.25	2.30	2.35
E1	Edge Lead Center to Center (axial)	---	1.00	---
E2	Edge Lead Center to Center (centerline)	---	1.75	---
e	Lead Finger (Pad to Pad) Pitch	---	0.50	---
f (e-b)	Lead Finger (Pad to Pad) Space	---	0.25	---
L	Lead Finger (Pad) Length	0.30	0.35	0.40
L'	Corner Lead Finger (Pad) Chamfer Length	---	0.105	---
L"	Corner Lead Finger (Pad) Short Side Length	---	0.245	---
r	Align Feature Dimension	---	0.250	---
x	Space Align Feature to Lead	---	0.20	---
s	Space Lead Finger to Package Edge	---	0.10 REF	---
w	Width Between Corner Leads	0.2	0.25	0.3
aaa	Package Edge Tolerance	---	0.05 REF	---
bbb	Mold Flatness	---	0 REF	---
ccc	Coplanarity	---	0.08 REF	---





7.1 PART NUMBER IDENTIFICATION

Product	Top Mark	
	Production Parts	Engineering Samples
ICG-1020S	G20S	“E” on the last line

For the latest packaging information, assembly recommendations and landing patterns (footprints), please refer to InvenSense MEMS Handling Application Note.

8. REGISTER MAP

The register map for the ICG-1020S is listed below.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02	02	DLPF_b1_H_Yaxis	R/W	DLPF_b1_int_Y[1:0]		DLPF_b1_float_Y[13:8]					
09	09	DLPF_b1_L_Yaxis	R/W	DLPF_b1_float_Y[7:0]							
0E	14	DLPF_b0b2_H_Xaxis	R/W	DLPF_b0b2_int_X[1:0]		DLPF_b0b2_float_X[13:8]					
0F	15	DLPF_b0b2_L_Xaxis	R/W	DLPF_b0b2_float_X[7:0]							
10	16	DLPF_b1_H_Xaxis	R/W	DLPF_b1_int_X[1:0]		DLPF_b1_float_X[13:8]					
11	17	DLPF_b1_L_Xaxis	R/W	DLPF_b1_float_X[7:0]							
12	18	DLPF_b0b2_H_Yaxis	R/W	DLPF_b0b2_int_Y[1:0]		DLPF_b0b2_float_Y[13:8]					
13	19	XG_OFFS_USRH	R/W	X_OFFS_USR[15:8]							
14	20	XG_OFFS_USRL	R/W	X_OFFS_USR[7:0]							
15	21	YG_OFFS_USRH	R/W	Y_OFFS_USR[15:8]							
16	22	YG_OFFS_USRL	R/W	Y_OFFS_USR[7:0]							
19	25	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	-	HPF_Order[1:0]		HPF_CFG[2:0]			DLPF_CFG[1:0]	
1B	27	GYRO_CONFIG	R/W	XG_ST	YG_ST	-	FS_SEL [1:0]		-	-	FCHOICE_B
26	38	HPF_DLPF_Rst_AZ	R/W	-	-	-	-	-	HPF_AZ	HPF_Reset	DLPF_Reset
37	55	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	-	-	-	-
38	56	INT_ENABLE	R/W	-	-	-	-	-	-	-	DATA_RDY_EN
3A	58	INT_STATUS	R	-	-	-	-	-	-	-	DATA_RDY_INT
41	65	TEMP_OUT_H	R	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	R	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	R	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	R	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	R	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	R	GYRO_YOUT[7:0]							
6A	106	USER_CTRL	R/W	-							SIG_COND_RST
6B	107	PWR_MGMT_1	R/W	DEVICE_RESET	SLEEP	-	-	-	CLKSEL[2:0]		
70	112	DLPF_b0b2_L_Yaxis	R/W	DLPF_b0b2_float_Y[7:0]							
71	113	DLPF_a1_H	R/W	DLPF_a1_int[1]		DLPF_a1_float[13:8]					
72	114	DLPF_a1_L	R/W	DLPF_a1_float[7:0]							
73	115	DLPF_a2_H	R/W	DLPF_a2_int[1:0]		DLPF_a2_float[13:8]					
74	116	DLPF_a2_L	R/W	DLPF_a2_float[7:0]							
75	117	WHO_AM_I	R	-	WHO_AM_I[6:1]						-
76	118	SPI_SEL	R/W	-	-	-	-	SPI_mode	-		-

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the GYRO_XOUT_H register (Register 67) contains the 8 most significant bits, *GYRO_XOUT*[15:8], of the 16-bit X-Axis gyroscope measurement, *GYRO_XOUT*.

9. REGISTER DESCRIPTIONS

This section describes the function and contents of each register.

9.1 REGISTERS 02, 09, 14-18, 112-116 - X AND Y AXES DIGITAL LOW PASS FILTER COEFFICIENTS

DLPF_B1_H_YAXIS, DLPF_B1_L_YAXIS, DLPF_B0B2_H_XAXIS, DLPF_B0B2_L_XAXIS
DLPF_B1_H_XAXIS, DLPF_B1_L_XAXIS, DLPF_B0B2_H_YAXIS, DLPF_B0B2_L_YAXIS
DLPF_A1_H, DLPF_A1_L, DLPF_A2_H, DLPF_A2_L

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02	02	DLPF_b1_H_Yaxis	DLPF_b1_int_Y[1:0]		DLPF_b1_float_Y[13:8]					
09	09	DLPF_b1_L_Yaxis	DLPF_b1_float_Y[7:0]							
0E	14	DLPF_b0b2_H_Xaxis	DLPF_b0b2_int_X[1:0]		DLPF_b0b2_float_X[13:8]					
0F	15	DLPF_b0b2_L_Xaxis	DLPF_b0b2_float_X[7:0]							
10	16	DLPF_b1_H_Xaxis	DLPF_b1_int_X[1:0]		DLPF_b1_float_X[13:8]					
11	17	DLPF_b1_L_Xaxis	DLPF_b1_float_X[7:0]							
12	18	DLPF_b0b2_H_Yaxis	DLPF_b0b2_int_Y[1:0]		DLPF_b0b2_float_Y[13:8]					
70	112	DLPF_b0b2_L_Yaxis	DLPF_b0b2_float_Y[7:0]							
71	113	DLPF_a1_H	DLPF_a1_int[1]		DLPF_a1_float[13:8]					
72	114	DLPF_a1_L	DLPF_a1_float[7:0]							
73	115	DLPF_a2_H	DLPF_a2_int[1:0]		DLPF_a2_float[13:8]					
74	116	DLPF_a2_L	DLPF_a2_float[7:0]							

Description:

The DLPF can be configured to have different corner frequencies as shown in table below. The default -3dB corner frequency is set at 250Hz. The “b” coefficients are axis specific, while “a” coefficients are common to both axes (X and Y). Also “b0” and “b2” coefficients are equal and have been combined into a single coefficient “b0b2”. The format of these coefficients is 2 bits integer plus 14 bits floating point. They are represented in 2’s complement format.

	Parameter Value (Hex)				
-3dB Corner Freq.	40/160 Hz	80/320 Hz	160/640 Hz	250 Hz	500 Hz
DLPF_b0b2_Yaxis	0x0004	0x0011	0x0040	0x0095	0x0212
DLPF_b1_Yaxis	0x0008	0x001C	0x006D	0x0100	0x0387
DLPF_b0b2_Xaxis	0x0004	0x0011	0x0040	0x0095	0x0212
DLPF_b1_Xaxis	0x0008	0x001C	0x006D	0x0100	0x0387
DLPF_a1	0x82D7	0x85AF	0x8B59	0x91AE	0xA2EE
DLPF_a2	0x3D38	0x3A8F	0x3594	0x307C	0x24BD

Parameters:

DLPF_b0b2_Yaxis 16-bit b0 & b2 (b0=b2) coefficients of DLPF for Y-axis
DLPF_b1_Yaxis 16-bit b1 coefficient of DLPF for Y-axis
DLPF_b0b2_Xaxis 16-bit b0 & b2 (b0=b2) coefficients of DLPF for X-axis
DLPF_b1_Xaxis 16-bit b1 coefficient of DLPF for X-axis
DLPF_a1 16-bit a1 coefficient of DLPF for both X and Y axes
DLPF_a2 16-bit a2 coefficient of DLPF for X both and Y axes

9.2 REGISTERS 19 TO 22 – GYROSCOPE OFFSET ADJUSTMENT

XG_OFFS_USRH, XG_OFFS_USRL, YG_OFFS_USRH, YG_OFFS_USRL

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13	19	XG_OFFS_USRH	X_OFFS_USR[15:8]							
14	20	XG_OFFS_USRL	X_OFFS_USR[7:0]							
15	21	YG_OFFS_USRH	Y_OFFS_USR[15:8]							
16	22	YG_OFFS_USRL	Y_OFFS_USR[7:0]							

Description:

These registers are used to remove DC bias from the sensor outputs. The values in these registers are subtracted from the gyroscope sensor values before going into the sensor registers (see registers 67 to 70). Resolution of each bit is 21 mdps per bit.

Parameters:

XG_OFFS_USR_H/L 16-bit offset of X gyroscope (2's complement)

YG_OFFS_USR_H/L 16-bit offset of Y gyroscope (2's complement).

9.3 REGISTER 25 – SAMPLE RATE DIVIDER

SMPRT_DIV

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	25	SMPLRT_DIV	SMPLRT_DIV[7:0]							

Description:

This register specifies the divider from the gyroscope output rate that can be used to generate a reduced Sample Rate. When this register is effective, the Sample Rates are shown in table below:

FCHOICE_B	SMPLRT_DIV	Sample Rate	DLPF_CFG	-3dB Corner Frequency (Hz)
0	≥0	8 kHz / (SMPLRT_DIV+1)	0x (DLPF bypassed)	3600
			10 (DLPF Enabled)	40, 80, 160, 250, 500
1	≥1	8 kHz / SMPLRT_DIV	0x (DLPF bypassed)	4000
			10 (DLPF Enabled)	160, 320, 640
1	0	32 kHz	0x (DLPF bypassed)	8900
			10 (DLPF Enabled)	160, 320, 640

Parameters:

SMPLRT_DIV 8-bit unsigned value. The Sample Rate is determined by dividing the gyroscope output rate by this value.

9.4 REGISTER 26 – CONFIGURATION

CONFIG

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1A	26	CONFIG	-	HPF_Order[1:0]		HPF_CFG[2:0]			DLPF_CFG[1:0]	

Description:

Please refer to section 8 on how to set the HPF parameters and description of the "m" factor.

HPF_Order[1:0]		10	11
HPF_CFG[2:0]	"m" factor	-3dB corner (Hz)	-3dB corner (Hz)
000	9	10	15
001	11	2.5	3.75
010	12	1.25	1.872
011	13	0.625	0.936
100	14	0.312	0.468
101	15	0.156	0.234
110	16	0.078	0.117
111	17	0.039	0.059

Parameters:

HPF_Order[1:0]
0x – Bypass high-pass filters
10 – Select one high-pass filter
11 – Select two high-pass filters in series (2nd order high-pass)

HPF_CFG[2:0]
Selects the "m" factor, which determines high-pass filter -3dB corner frequency.(see section 8)

DLPF_CFG[1:0]
0x – Bypass DLPF
10 – Select to enable DLPF

9.5 REGISTER 27 – GYROSCOPE CONFIGURATION

GYRO_CONFIG

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	27	GYRO_CONFIG	XG_ST	YG_ST	-	FS_SEL [1:0]		-	-	FCHOICE_B

Description:

This register is used to trigger gyroscope self test and configure the gyroscopes' full scale range.
Gyroscope self-test permits users to test the mechanical and electrical portions of the gyroscope. When self-test is activated by setting XG_ST, YG_ST bits in register 27, the on-board electronics will actuate the appropriate sensor. This actuation will move the sensor's proof masses over a distance equivalent to a pre-defined Coriolis force. This proof mass displacement results in a change in the sensor output, which is reflected in the output signal. The output signal is used to observe the self-test response. The self-test response (STR) is stored in the sensor data output registers 67 – 70. This self-test-response is used to determine whether the part has passed or failed self-test
This self-test response must be within the limits provided in product specification document for the part to pass self-test. Otherwise, the part is deemed to have failed self-test.

FS_SEL selects the full scale range of the gyroscope outputs according to the following table.

FS_SEL	Full Scale Range
0	± 46.5 °/s
1	± 93 °/s
2	± 187 °/s
3	± 374 °/s

FCHOICE_B, in conjunction with *DLPF_CFG* (Register 26), and SMPLRT_DIV (Register 25) is used to choose the gyroscope output settings, such as filter bandwidth and sample rate, as described in register 25 (SMPRT_DIV) section.
Bit 5 and 1-2 are reserved.

Parameters:

XG_ST	Setting this bit causes the X axis gyroscope to perform self test.
YG_ST	Setting this bit causes the Y axis gyroscope to perform self test.
FS_SEL	2-bit unsigned value. Selects the full scale range of gyroscopes.
FCHOICE_B	1-bit unsigned value used to choose the gyroscope output setting.

9.6 REGISTER 38 – DLPF AND HPF RESET AND AUTO ZERO

HPF_DLPF_Rst_AZ

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26	38	HPF_DLPF_Rst_AZ	R/W	-	-	-	-	-	HPF_AZ	HPF_Reset	DLPF_Reset

Description:

Both High Pass Filter (HPF) and Low Pass Filter (DLPF) can be reset. In addition, HPF can be Auto Zeroed.
In case of HPF, the reset command clears the HPF filter state, while the auto-zero command loads the filter state with filter input. This will result in the following response for a filter input of DCin+ACin (an input with DC and AC components):

a) HPF output prior to reset or Auto Zero (AZ) → ACin
b) HPF output right after reset → DCin+ACin
c) HPF output right after AZ → 0

Please refer to section 8 on how to set the HPF.

Parameters:

HPF_AZ When this bit is equal to 1, HPF is Auto Zeroed.

HPF_Reset When this bit is equal to 1, HPF is reset.

DLPF_Reset When this bit is equal to1, DLPF is reset.

9.7 REGISTER 55 – INT PIN / BYPASS ENABLE CONFIGURATION

INT_PIN_CFG

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37	55	INT_PIN_CFG	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	-	-	-	-

Description:

This register configures the behavior of the interrupt signals at the INT pins.

Parameters:

INT_LEVEL When this bit is equal to 0, the logic level for the INT pin is active high.
When this bit is equal to 1, the logic level for the INT pin is active low.

INT_OPEN When this bit is equal to 0, the INT pin is configured as push-pull.
When this bit is equal to 1, the INT pin is configured as open drain.

LATCH_INT_EN When this bit is equal to 0, the INT pin emits a 50us long pulse.
When this bit is equal to 1, the INT pin is held high until the interrupt is cleared.

INT_RD_CLEAR When this bit is equal to 0, interrupt status bits are cleared only by reading INT_STATUS (Register 58)
When this bit is equal to 1, interrupt status bits are cleared on any read operation.

9.8 REGISTER 56 – INTERRUPT ENABLE

INT_ENABLE

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38	56	INT_ENABLE	-	-	-	-	-	-	-	DATA _RDY_EN

Description:

Bits 7 through 1 are reserved.

Parameters:

DATA_RDY_EN When set to 1, this bit enables the Data Ready interrupt. The Data Ready interrupt is triggered when all the sensor registers have been written with the latest gyro sensor data.

9.9 REGISTER 58 – INTERRUPT STATUS

INT_STATUS

Type: Read Only

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3A	58	INT_STATUS	-	-	-	-	-	-	-	DATA _RDY_INT

Description:

This register shows the interrupt status when gyro data is ready to be read. This bit will clear after the register is read.
Bits 7 through 1 are reserved.

Parameters:

DATA_RDY_INT This bit automatically sets to 1 when a Data Ready interrupt is generated.
The bit clears to 0 after the register has been read.

9.10 REGISTERS 65 AND 66 – TEMPERATURE MEASUREMENT

TEMP_OUT_H and TEMP_OUT_L

Type: Read Only

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41	65	TEMP_OUT_H	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	TEMP_OUT[7:0]							

Description:

These registers store the most recent temperature sensor measurement.
Temperature measurements are written to these registers at the Sample Rate as defined in Register 25.
These temperature measurement registers, along with the gyroscope measurement registers, are composed of two sets of registers: an internal register set and a user-facing read register set.
The data within the temperature sensor's internal register set is always updated at the Sample Rate. Meanwhile, the user-facing read register set duplicates the internal register set's data values whenever the serial interface is idle. This guarantees that a burst read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt.
The range of temperatures covered by this sensor register is from -123C to +123C.

Parameters:

TEMP_OUT 16-bit signed value.
Stores the most recent temperature sensor measurement.

9.11 REGISTERS 67 TO 70 – GYROSCOPE MEASUREMENTS

GYRO_XOUT_H, GYRO_XOUT_L, GYRO_YOUT_H, and GYRO_YOUT_L

Type: Read Only

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43	67	GYRO_XOUT_H	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	GYRO_YOUT[7:0]							

Description:

These registers store the most recent gyroscope measurements. Gyroscope measurements are written to these registers at the Sample Rate as defined in Register 25.

The gyroscope sensor registers continuously update at the user selectable ODR sample rate whenever the serial interface is idle. It is recommended to use burst reads on host interface to guarantee a read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt. Failing to do so, may result in reading the low and high byte of the same sensor from different samples which could appear as noise peaks to the user for example. The following should be considered for single byte read mode:

1. Data_RDY_INT gets generated any time the sensor registers get updated with the sensor data. The frequency of this interrupt is the same as the ODR which is user selectable. The INT Configurations, INT status register and INT pin can be configured using the user register 37h, 38h and 3Ah.
2. The sensor register outputs are 16 bits (2 bytes). Both bytes should be read at the same time in order to get reliable data using burst mode. If a single byte read is used, the host needs to read the bytes back to back after Data_RDY_INT is set to ensure both bytes are from same sample.
3. The sensor registers should be read at a faster rate than the selected ODR with the read cycle preferably completed for all the sensors to get consistent and reliable output.

Each 16-bit gyroscope measurement has a full scale defined in *FS_SEL* (Register 27). For each full scale setting, the gyroscopes' sensitivity per LSB in *GYRO_xOUT* is shown in the table below:

FS_SEL	Full Scale Range	LSB Sensitivity
0	± 46.5 °/s	700 LSB/°/s
1	± 93 °/s	350 LSB/°/s
2	± 187 °/s	175 LSB/°/s
3	± 374 °/s	87.5 LSB/°/s

Parameters:

GYRO_XOUT 16-bit 2's complement value.
Stores the most recent X axis gyroscope measurement.

GYRO_YOUT 16-bit 2's complement value.
Stores the most recent Y axis gyroscope measurement.

9.12 REGISTER 107 – POWER MANAGEMENT 1

PWR_MGMT_1

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6B	107	PWR_MGMT_1	DEVICE _RESET	SLEEP	-	-	-	CLKSEL[2:0]		

Description:

This register allows the user to configure the power mode and clock source. It also provides a bit for resetting the entire device, and a bit for disabling the temperature sensor.

By setting *SLEEP* to 1, the device can be put into low power sleep mode.

An internal 20MHz oscillator or the gyroscope based clock (PLL) can be selected as the device clock source. The PLL is the default clock source upon power up. In order for the gyroscope to perform to spec, the PLL must be selected as the clock source.

When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscopes disabled. However, this is only recommended if the user wishes to use the internal temperature sensor in this mode.

The clock source can be selected according to the following table.

CLKSEL	Clock Source
0	Internal 20MHz oscillator
1	PLL
2	PLL
3	PLL
4	PLL
5	PLL
6	Internal 20MHz oscillator
7	Reserved

For further information regarding the device clock source, please refer to the relevant Product Specification document.

Bits 5 through 3 are reserved.

Parameters:

DEVICE_RESET When set to 1, this bit resets all internal registers to their default values. The bit automatically clears to 0 once the reset is done.

SLEEP When set to 1, this bit puts the device into sleep mode.

CLKSEL 3-bit unsigned value. Specifies the clock source of the device.

9.13 REGISTER 117 – WHO AM I

WHO_AM_I

Type: Read Only

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75	117	WHO_AM_I	-	WHO_AM_I[5:0]						-

Description:

This register is used to verify the identity of the device.

The default value of the register is 0x88.

Bits 0 and 7 are reserved.

Parameters:

WHO_AM_I Contains the 6-bit device identifier.

9.14 REGISTER 118 – SPI BUS SELECTION

SPI_SEL

Type: Read/Write

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
76	118	SPI_SEL	-	-	-	-		SPI_mode	-	-

Description:

The default value of this register is 0 which corresponds to 4-wire SPI. Setting this bit to 1 enables the 3-wire SPI operation.
Bits 0 to 1 and bits 3 to 7 are reserved.

Parameters:

SPI_mode When set to 1, this bit enables 3-wire SPI operation.
The default value of zero corresponds to 4-wire SPI.

10. HIGH PASS FILTER, HLPF, SETTING PIN DESCRIPTION

As mentioned, the purpose of high-pass filters is to attenuate or eliminate the effect of slow varying offset that may result from the gyro or the substrate PCB warp due to heat. The customer can choose from 1st or 2nd order high-pass filter of varying bandwidths. The digital high-pass filter transfer function for each individual filter can be described in Z-domain as $H_{hpf}(z) = \frac{z-1}{z-1+2^{-m}}, where\ m = 9,11,12,13,14,15,16,17$

The filter phase delay can be computed from

$$\theta(f) = tan^{-1}\left(\left.\sin\left(\frac{2\pi f}{f_s}\right)\right/\cos\left(\frac{2\pi f}{f_s}\right) - 1\right) - tan^{-1}\left(\left.\sin\left(\frac{2\pi f}{f_s}\right)\right/\cos\left(\frac{2\pi f}{f_s}\right) - 1 + 2^{-m}\right)$$

While the group delay is calculated by this equation, $\frac{\theta(f)}{360^0}/f_s$, where f_s is equal to 8kHz.

Corner frequency selection for all HPF settings can be found in table, located in register map section.

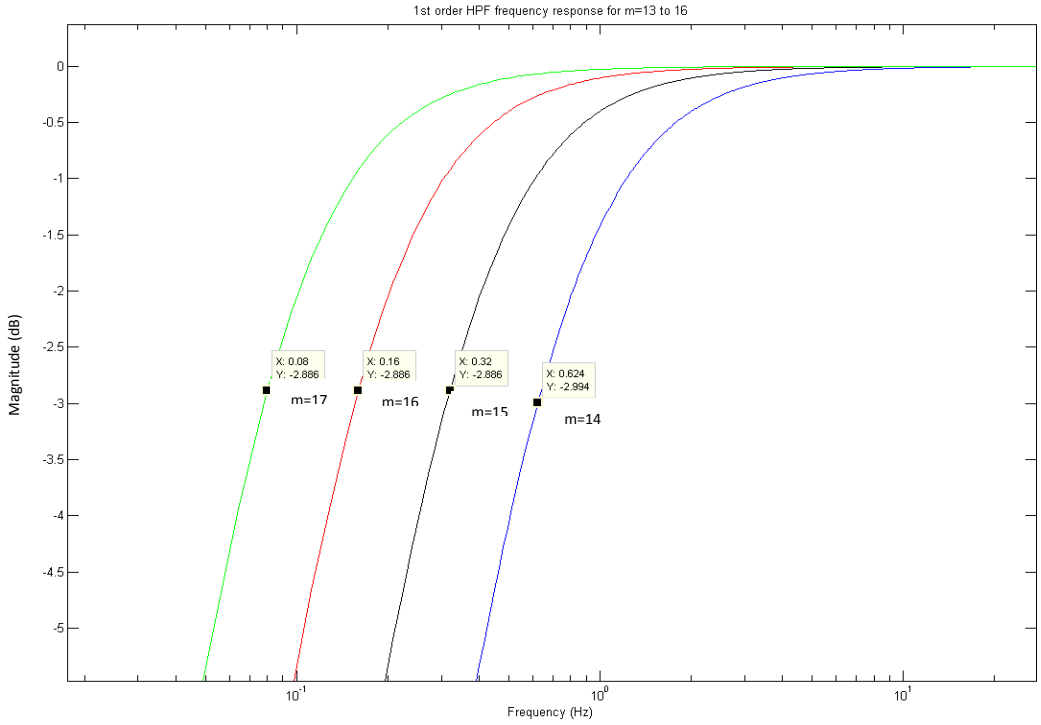


Figure 7. 1st order HPF frequency response for coefficient m=13,14,15,16

The high pass filter(s) can also be reset or auto-zeroed by writing and then clearing HPF_reset and HPF_AZ bits in User register space. The reset command clears the HPF filter state, while the auto-zero command loads the filter state with filter input. This will result in the following response for a filter input of DCin+ACin:

a) HPF output prior to reset or AZ → ACin
b) HPF output immediately after reset → DCin+ACin
c) HPF output immediately after auto-zero → 0

The choice of HPF (bypass, 1st order or 2nd order) is selected by programming HPF_Order[1:0] bits.
The HPF filter corner ("m"-coefficient) can be selected by programming HPF_CFG[2:0].

11. REVISION HISTORY

REVISION DATE	REV NUMBER	DESCRIPTION
07/01/2016	1.0	Initial Release

COMPLIANCE DECLARATION DISCLAIMER

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