Kintex-7 FPGA KC724 GTX Transceiver Characterization Board

User Guide

UG932 (v2.2) October 10, 2014

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/10/2012	1.0	Initial Xilinx release.
7/29/2013	2.0	Updated Table 1-15 and Appendix B, Master Constraints File Listing.
12/13/2013	2.1	Updated disclaimer and copyright. Updated Table 1-6, Table 1-7, Table 1-8, Table 1-9, Table 1-10, Table 1-11, Table 1-15, and Table 1-16.
10/10/2014	2.2	Updated first paragraph and modified vendor list in 7 Series GTX Transceiver Power Module. Removed vendor list from References.

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Appendix E: Regulatory and Compliance Information

Chapter 1

KC724 Board Features and Operation

This chapter describes the components, features, and operation of the KC724 Kintex®-7 FPGA GTX Transceiver Characterization Board. The KC724 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Kintex-7 XC7K325T-3 FFG900E FPGA. The KC724 board schematic, bill-of-material (BOM), layout files, and reference designs are available online at:

Kintex-7 FPGA KC724 Characterization Kit website

KC724 Board Features

- Kintex-7 XC7K325T-3 FFG900E FPGA
- Onboard power supplies for all necessary voltages
- Terminal blocks for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ SD controller
- Power module supporting Kintex-7 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Four Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Two VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I2C bus
- PMBus connectivity to onboard digital power supplies
- Active cooling for the FPGA

The KC724 board block diagram is shown in Figure 1-1.

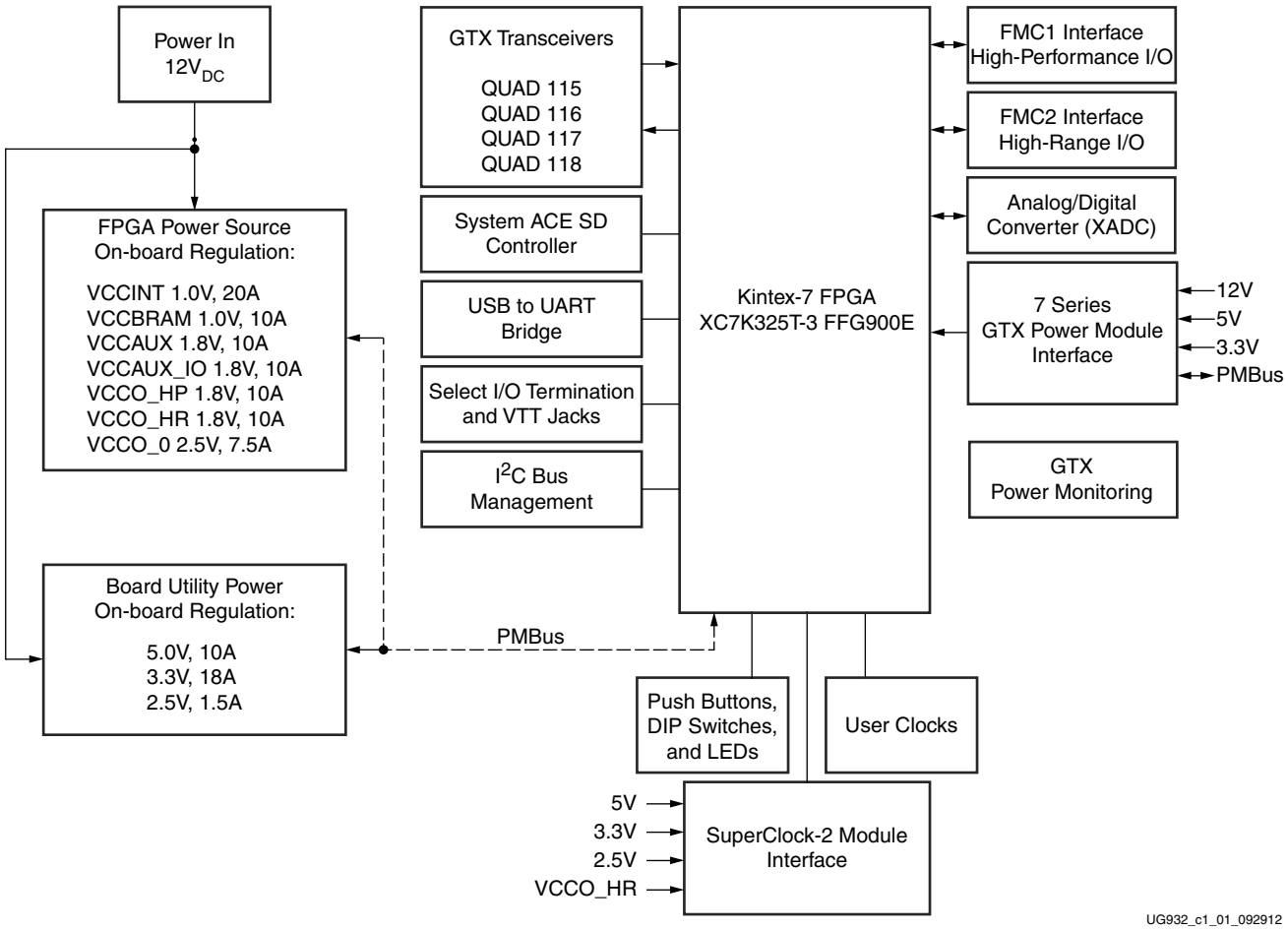

Figure 1-1: **KC724 Board Block Diagram**

Detailed Description

Figure 1-2 shows the KC724 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Caution! The KC724 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

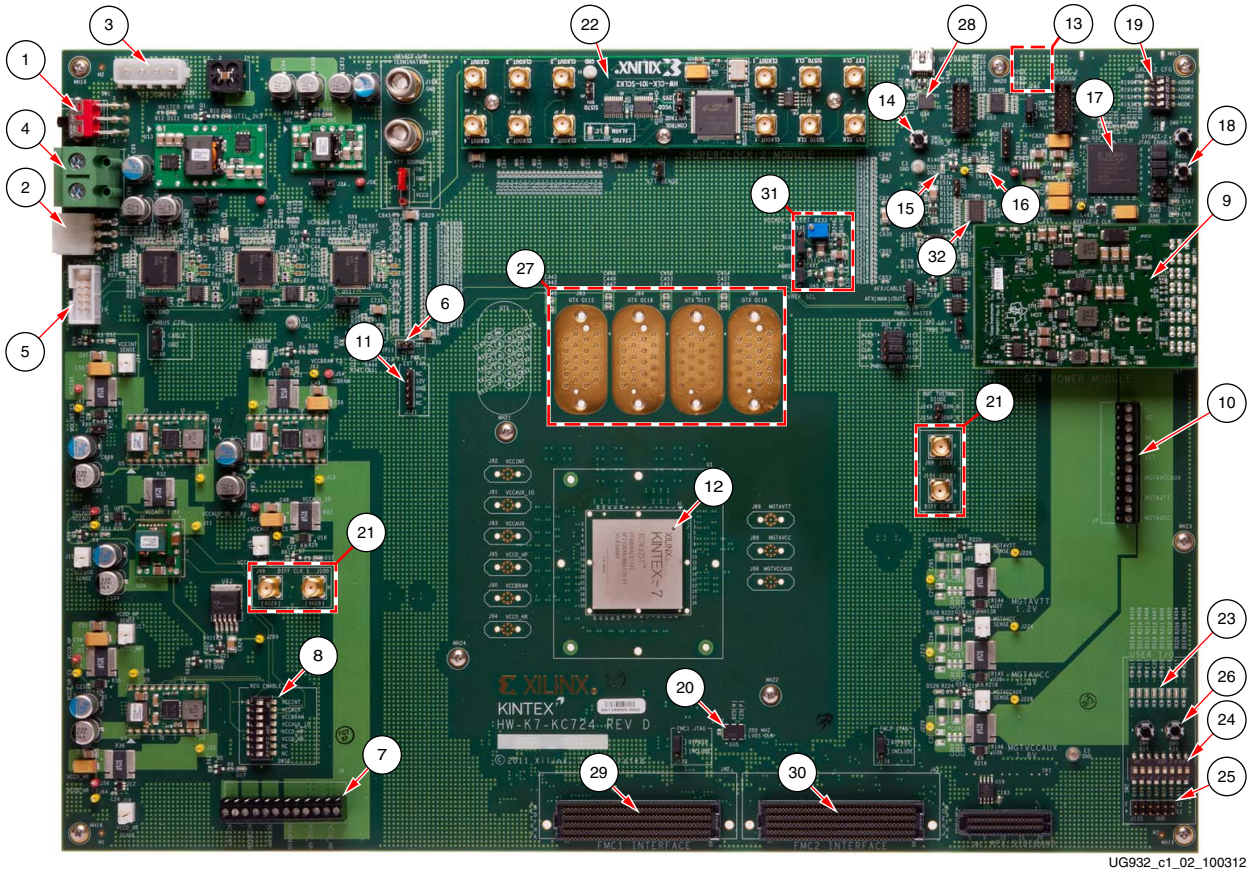

Figure 1-2: **KC724 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **KC724 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	SW1	Power Switch, page 9
2	J2	12V Mini-Fit Connector, page 9
3	J131	12V ATX Connector, page 9
4	J5	12V Euro-Mag Connector, page 9
5	J26	TI PMBus cable connector, page 13
6	J27	Regulation inhibit connector, page 13
7	J6	Core power terminal block (see Using External Power Sources, page 12)
8	SW10	Core power regulator enable switches, page 13
9		7 Series GTX Transceiver Power Module, page 14
10	J7	GTX transceiver power terminal block, page 15
11	J121	Active Heatsink Power Connector, page 16
12	U1	Kintex-7 XC7K325T-3 FFG900E FPGA, page 17
13	U8	USB JTAG configuration port (Digilent module), page 17
14	SW3	PROG_B Push Button, page 18
15	DS21	DONE LED, page 18
16	DS25	INIT LED, page 19
17	U32	System ACE SD Controller, page 19
18	SW7	System ACE SD Controller Reset, page 19
19	SW8	System ACE SD Configuration Address DIP Switches, page 19
20	U35	200 MHz 2.5V LVDS Oscillator, page 20
21	J98, J99, J100, J101	Differential SMA MRCC Pin Inputs, page 20
22		SuperClock-2 Module, page 20
23	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (Active High), page 22
24	SW2	User DIP Switches (Active High), page 22
25	J125	User Test I/O, page 22
26	SW4, SW5	User Push Buttons (Active High), page 23
27	J83, J84, J85, J86	GTX transceiver connector pads, page 23
28	U34	USB-to-UART Bridge, page 28
29	JA2	FMC1 Connector, page 29
30	JA3	FMC2 Connector, page 29

Table 1-1: **KC724 Board Feature Descriptions *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
31		XADC, page 40
32	U39	I2C Bus Management, page 41

Power Management

Callouts 1 through 11 shown in Figure 1-2 refer to components associated with the board's power management system.

Board Power and Switch

The KC724 board is powered through J2 (callout 2, Figure 1-2) using the 12V AC adapter included with the board. J2 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

Caution! When powering the board through J2, use only the power supply provided for use with this board (Xilinx part number 3800033).

Caution! Do **NOT** plug a PC ATX power supply 6-pin connector into J2 on the KC724 board. The ATX 6-pin connector has a different pinout than J2. Connecting an ATX 6-pin connector into J2 will damage the KC724 board and void the board warranty.

Power can also be provided through:

- Connector J131 which accepts an ATX hard disk 4-pin power plug
- Euro-Mag terminal block J5 which can be used to connect to a bench-top power supply

Caution! Because terminal block J5 provides no reverse polarity protection, use a power supply with a current limit set at 5A max.

Caution! Do NOT apply power to J2 and connectors J131 and/or J5 at the same time. Doing so will damage the KC724 board.

The KC724 board power is turned on or off by switch SW1 (callout 1, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates.

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

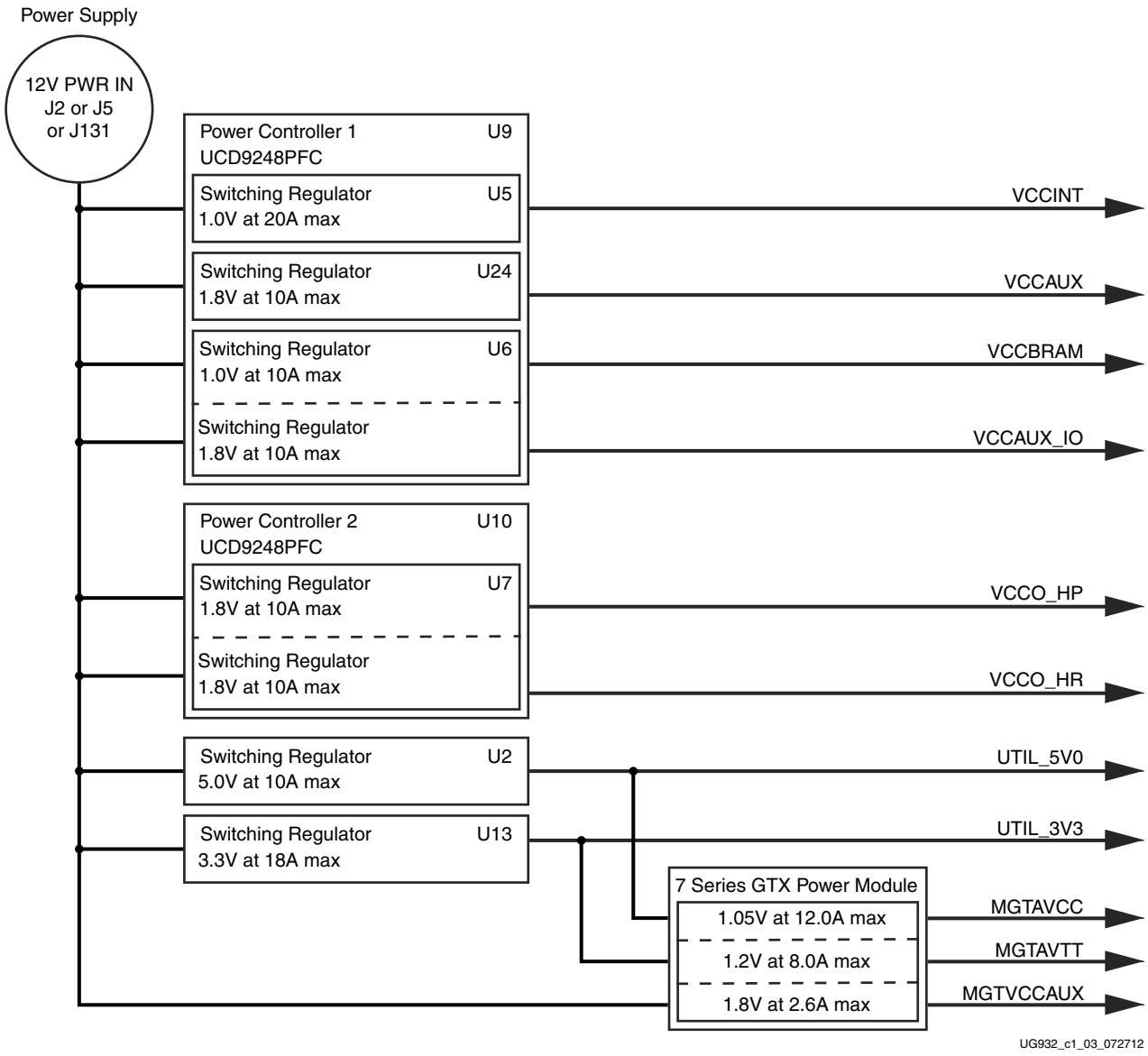

Figure 1-3: **KC724 Board Power Supply Block Diagram**

The KC724 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage
Core voltage controller and regulators				
UCD9248PFC	U9	PMBus compliant digital PWM system controller (Address = 52)		
PTD08D210W	U5	Adjustable switching regulator dual 10A, 0.6V to 3.6V	VCCINT	1.0V
PTD08A010W	U24	Adjustable switching regulator 10A, 0.6Vto 3.6V	VCCAUX	1.8V
PTD08D210W (V_{OUT} A)	U6	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCCBRAM	1.0V
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCCAUX_IO	1.8V
UCD9248PFC	U10	PMBus compliant digital PWM system controller ((Addr = 53)		
PTD08D210W (V_{OUT} A)	U7	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC_HP	1.8V
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC_HR	1.8V
UCD9248PFC(1)	U11	PMBus compliant digital PWM system controller (Address = 54)		
Utility switching regulators				
PTH12060W	U2	Adjustable switching regulator 10A, 1.2V to 5.5V	UTIL_5V0	5.0V
PTH12020W	U13	Adjustable switching regulator 18A, 1.2V to 5.5V	UTIL_3V3	3.3V
Linear regulators				
TL1963A	U47	Adjustable LDO Regulator 1.5A	UTIL_2V5	2.5V
TPS75925	U62	Fixed LDO regulator, 7.5A	VCCO_0	2.5V
ADP123	U21	Adjustable LDO Regulator, 300mA	VCC_1V2	1.2V
ADP123	U43	Adjustable LDO Regulator, 300mA	VCCADC_ADP	1.8V
REF3012	U45	Fixed LDO regulator, 25 mA	VREF_3012	1.25V

Notes:
1. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC, MGTAVTT, and MGTVCCAUX rail voltage and current levels through the TI Fusion test application.

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-2. If a design exceeds this value on any core power rail, power for that rail must be supplied externally through the 12-position core power terminal block J6 (callout 7, Figure 1-2) using a supply capable of providing the required current.

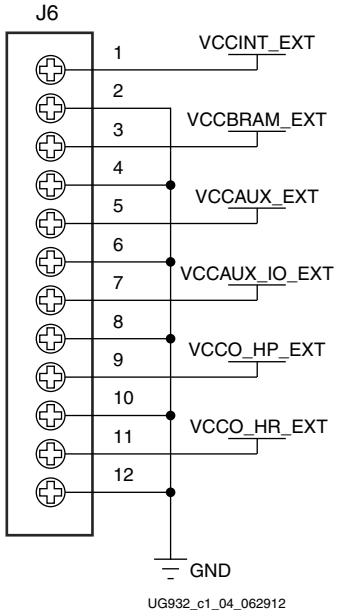

Figure 1-4: **Core Power Terminal Block**

Caution! The SW10 power regulator enable switch (callout 8, Figure 1-2) (see Disabling Onboard Power) must be set to the OFF position before turning ON the main power switch (SW1) and applying external power to the corresponding rail input pin on the core power terminal block J6 (callout 7, Figure 1-2).

Caution! The core power terminal block J6 has a maximum load current contact rating of 24A.

Disabling Onboard Power

Each core power regulator can be disabled through the 8-position regulator enable DIP switch, SW10 as shown in Figure 1-5. A switch in the ON position means the rail is supplied by an onboard regulator. Setting a switch in the opposite (OFF) position disables onboard power for that rail. SW10 is shown in Figure 1-2 as callout 8.

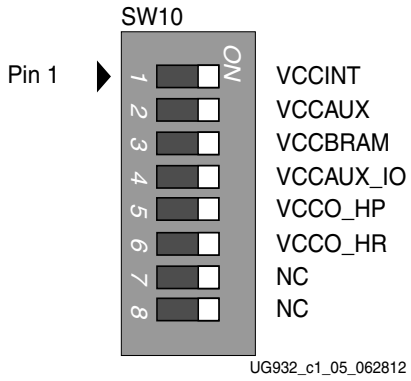

Figure 1-5: **Core Power Regulator Enable Switches**

Note: All onboard power can be disabled by placing a jumper across the TI PWR INH header J27 (callout 6, Figure 1-2). For the purposes of supplying external core power however, disabling onboard power through J27 would require the UTIL_5V0, UTIL_3V3 and UTIL_2V5 be supplied externally as well. The utility rails can be supplied through test points J58, J59 and J155, respectively.

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper and Switch Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, and U11 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J26 (callout 5, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the KC724 board are available from the Texas Instruments Digital Power website.

7 Series GTX Transceiver Power Module

The 7 series GTX transceiver power module (callout 9, Figure 1-2) supplies MGTAVCC, MGTAVTT, and MGTVCCAUX voltages to the FPGA GTX transceivers. Three 7 series GTX power modules from third-party vendors are provided with the KC724 board for evaluation. Any one of the three modules can be plugged into connectors J66 and J97 in the outlined and labeled power module location shown in Figure 1-6.

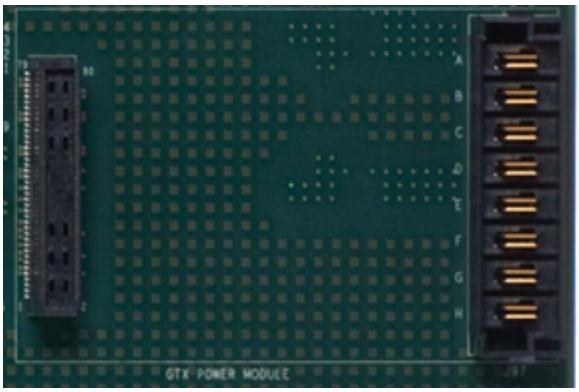

Figure 1-6: **Mounting Location, 7 Series GTX Transceiver Power Module**

Table 1-3 lists the nominal voltage values for the MGTAVCC, MGTAVTT and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by 7 series GTX modules included with the KC724 board.

Table 1-3: **7 Series GTX Transceiver Power Module**

Power Supply Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.05V	12A
MGTAVTT	1.2V	8A
MGTVCCAUX	1.8V	2.6A

The GTX transceiver power rails also have corresponding inputs on the GTX transceiver power terminal block J7 as shown in Figure 1-7 to supply each voltage independently from a bench-top power supply. J7 is shown in Figure 1-2 as callout 10.

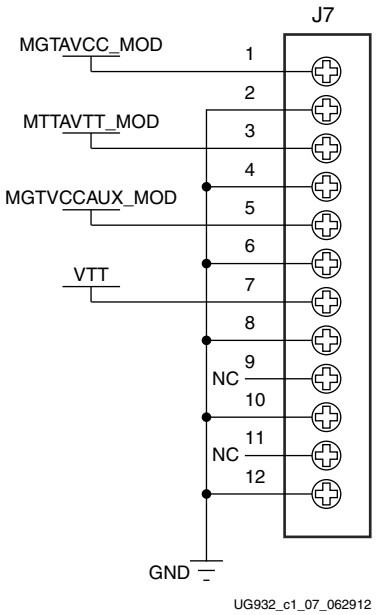

Figure 1-7: **GTX Transceiver Power Terminal Block**

Caution! The 7 series GTX Module **MUST** be removed when providing external power to the GTX transceiver rails.

Caution! The GTX transceiver power terminal block J7 has a maximum load current contact rating of 24A.

Information about the 7 series GTX power supply modules included with the KC724 kit is available from these vendor websites:

- Intersil
- Texas Instruments
- General Electric

Active Heatsink Power Connector

An active heatsink (Figure 1-8) is provided for the FPGA. A 12V fan is affixed to the heatsink and is powered from the 3-pin friction lock header J121 (Figure 1-9).

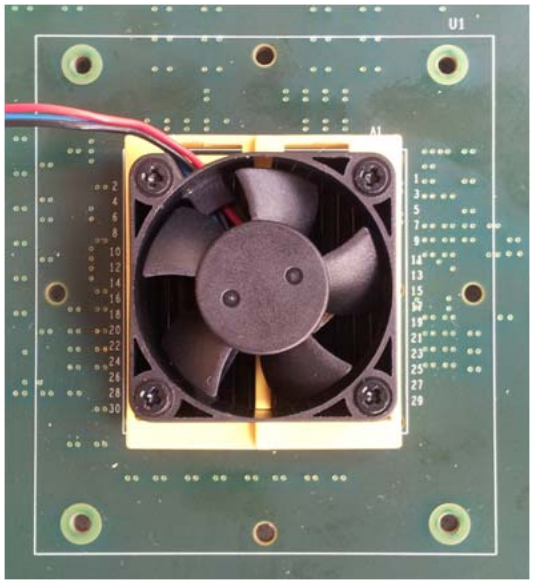

Figure 1-8: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-4:

Table 1-4: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-9 shows the heatsink fan power connector J121. J121 is shown in Figure 1-2 as callout 11.

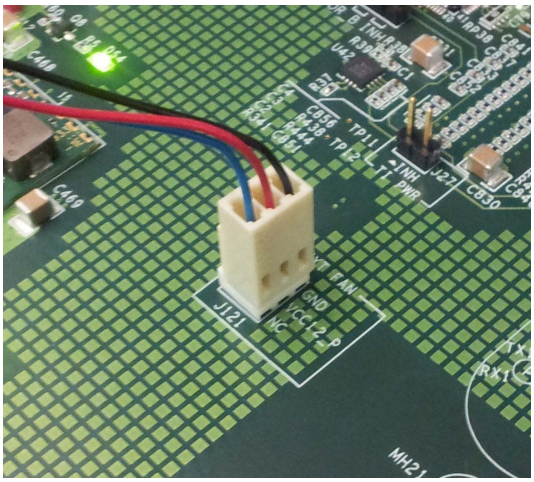

Figure 1-9: **Heatsink Fan Power Connector J121**

Kintex-7 FPGA

The KC724 board is populated with the Kintex-7 XC7K325T-3 FFG900E FPGA at U1 (callout 12, Figure 1-2). For further information on Kintex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 1].

FPGA Configuration

The FPGA is configured in JTAG mode only using one of the following options:

- USB JTAG configuration port (Digilent module)
- System ACE SD controller

The FPGA is configured through the Digilent onboard USB-to-JTAG configuration logic module (U8) where a host computer accesses the KC724 board JTAG chain through a standard-A plug to micro-B plug USB cable. (callout 13, Figure 1-2).

The FPGA is configured through the System ACE SD controller by setting the 4-bit configuration address DIP switch (SW8) to select one of eight bitstreams stored on a Secure Digital (SD) memory card (see System ACE SD Configuration Address DIP Switches, page 19).

The JTAG chain of the board is illustrated in Figure 1-10. By default only the Kintex-7 FPGA and the System ACE SD controller are part of the chain (J1 jumper OFF). Installing the J1 jumper adds the FMC interfaces as well.

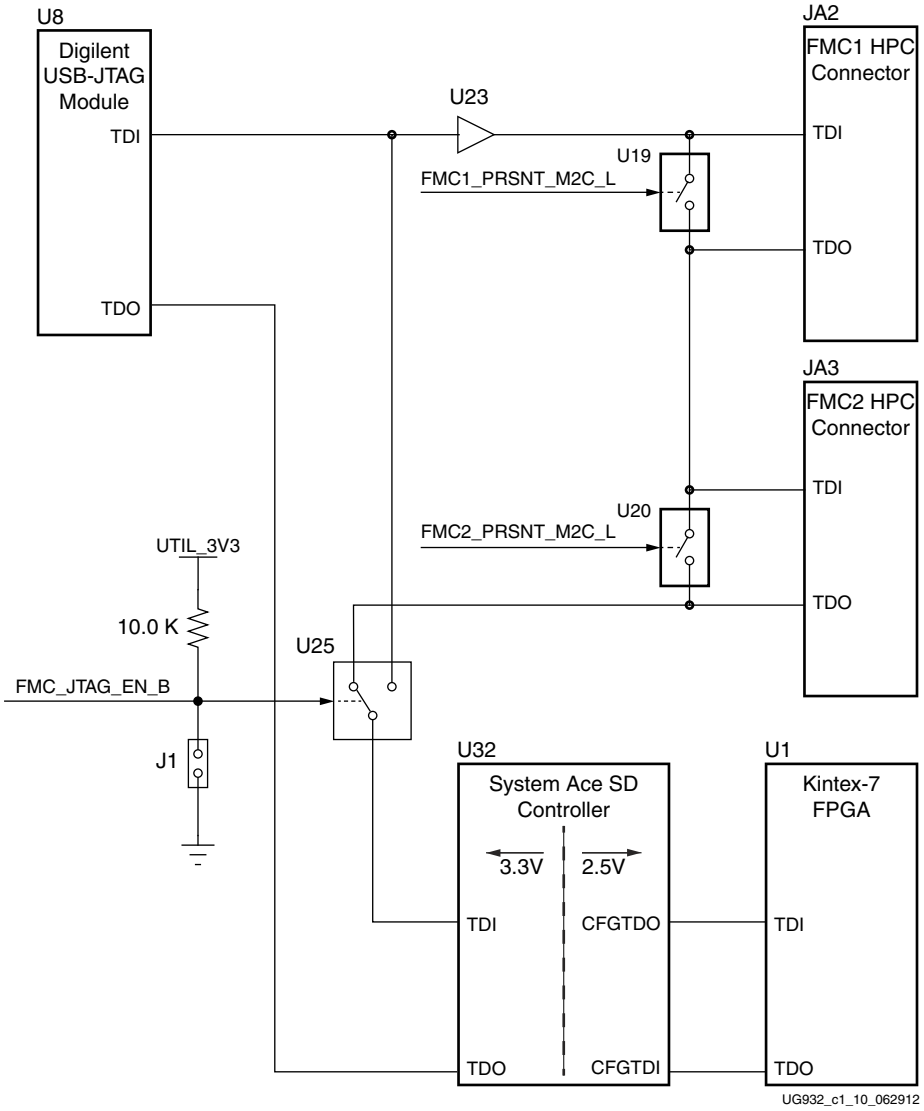

Figure 1-10: **JTAG Chain**

PROG_B Push Button

Pressing the PROG push button SW3 (callout 14, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 15, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 16, Figure 1-2) indicates the FPGA's initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE SD Controller

The onboard System ACE SD controller U32 (callout 17, Figure 1-2) allows storage of multiple configuration files on a Secure Digital (SD) card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector J8 located directly below the System ACE SD controller on the back side of the board.

System ACE SD Controller Reset

Pressing the SASD RESET push button SW7 (callout 18, Figure 1-2) resets the System ACE SD controller. The reset pin is an active-Low input.

System ACE SD Configuration Address DIP Switches

DIP switch SW8 shown in Figure 1-11 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW8 is shown in Figure 1-2 as callout 19.

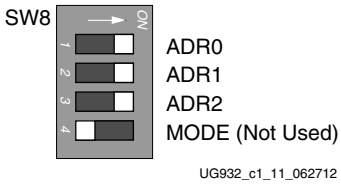

Figure 1-11: **Configuration Address DIP Switch (SW8)**

The switch settings for selecting each address are shown in Table 1-5.

Table 1-5: **SW8 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 20, Figure 1-2).

The KC724 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-6 lists the FPGA pin connections to the LVDS oscillator.

Table 1-6: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (U35)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
C25	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	200 MHz LVDS oscillator	Output
B25	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	201 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

Callout 21, Figure 1-2.

The KC724 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-7.

Table 1-7: **Differential SMA Clock Connections**

FPGA (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
AG29	USER CLOCK_1_P	Input	LVDS_25	CLK_DIFF_1_P	J99
AH29	USER CLOCK_1_N	Input	LVDS_25	CLK_DIFF_1_N	J100
D17	USER CLOCK_2_P	Input	LVDS_25	CLK_DIFF_2_P	J98
D18	USER CLOCK_2_N	Input	LVDS_25	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 22, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the KC724 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-8 shows the FPGA I/O mapping for the SuperClock-2 module interface. The KC724 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HR input power to the clock module interface.

Table 1-8: **SuperClock-2 FPGA I/O Mapping**

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
F11	Clock recovery	Input	LVDS_25	CM_LVDS1_P	1	Clock recovery	Output
E11	Clock recovery	Input	LVDS_25	CM_LVDS1_N	3	Clock recovery	Output
C12	Clock recovery	Input	LVDS_25	CM_LVDS2_P	9	Clock recovery	Output

Table 1-8: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
B12	Clock recovery	Input	LVDS_25	CM_LVDS2_N	11	Clock recovery	Output
AJ3	Clock recovery	Output	LVDS	CM_LVDS3_P	17	Clock recovery	Input
AK3	Clock recovery	Output	LVDS	CM_LVDS3_N	19	Clock recovery	Input
D26	Regional clock	Input	LVDS_25	CM_GCLK_P	25	Global clock	Output
C26	Regional clock	Input	LVDS_25	CM_GCLK_N	27	Global clock	Output
G30	Control I/O	In/Out	LVCMOS18	CM_CTRL_0	61	NC	–
H30	Control I/O	In/Out	LVCMOS18	CM_CTRL_1	63	NC	–
H27	Control I/O	In/Out	LVCMOS18	CM_CTRL_2	65	NC	–
H26	Control I/O	Output	LVCMOS18	CM_CTRL_3	67	DEC	Input
F30	Control I/O	Output	LVCMOS18	CM_CTRL_4	69	INC	Input
G29	Control I/O	Output	LVCMOS18	CM_CTRL_5	71	Align	Input
F27	Control I/O	In/Out	LVCMOS18	CM_CTRL_6	73	NC	–
G27	Control I/O	In/Out	LVCMOS18	CM_CTRL_7	75	NC	–
F28	Control I/O	In/Out	LVCMOS18	CM_CTRL_8	77	NC	–
G28	Control I/O	In/Out	LVCMOS18	CM_CTRL_9	79	LOL	
H25	Control I/O	Output	LVCMOS18	CM_CTRL_10	81	INT_ALRM	Input
H24	Control I/O	Output	LVCMOS18	CM_CTRL_11	83	C1B	Input
E30	Control I/O	Output	LVCMOS18	CM_CTRL_12	85	C2B	Input
E29	Control I/O	Output	LVCMOS18	CM_CTRL_13	87	C3B	Input
A30	Control I/O	Output	LVCMOS18	CM_CTRL_14	89	C1A	Input
B30	Control I/O	Output	LVCMOS18	CM_CTRL_15	91	C2A	Input
C30	Control I/O	In/Out	LVCMOS18	CM_CTRL_16	93	NC	–
D29	Control I/O	Output	LVCMOS18	CM_CTRL_17	95	CS0_C3A	Input
B29	Control I/O	Output	LVCMOS18	CM_CTRL_18	97	CS1_C4A	Input
C29	Control I/O	In/Out	LVCMOS18	CM_CTRL_19	99	NC	–
A26	Control I/O	In/Out	LVCMOS18	CM_CTRL_20	101	NC	–
A25	Control I/O	In/Out	LVCMOS18	CM_CTRL_21	103	NC	–
A28	Control I/O	In/Out	LVCMOS18	CM_CTRL_22	105	NC	–
B28	Control I/O	In/Out	LVCMOS18	CM_CTRL_23	107	NC	–
B24	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active High)

Callout 23, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-10 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-9: **User LEDs**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
A20	User LED	Output	LVCMOS18	APP_LED1	DS19
A17	User LED	Output	LVCMOS18	APP_LED2	DS20
A16	User LED	Output	LVCMOS18	APP_LED3	DS17
B20	User LED	Output	LVCMOS18	APP_LED4	DS18
C20	User LED	Output	LVCMOS18	APP_LED5	DS16
F17	User LED	Output	LVCMOS18	APP_LED6	DS15
G17	User LED	Output	LVCMOS18	APP_LED7	DS13
B17	User LED	Output	LVCMOS18	APP_LED8	DS14

User DIP Switches (Active High)

Callout 24, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-10. These pins can be used to set control pins or any other purpose. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 25, Figure 1-2.).

Table 1-10: **User DIP Switches**

FPGA (U1)				Schematic Net Name	DIP Switch Reference	J125 Test Header Pin
Pin	Function	Direction	IOSTANDARD			
E18	User switch	Input	LVCMOS18	USER_SW1	SW2	2
B19	User switch	Input	LVCMOS18	USER_SW2		4
C19	User switch	Input	LVCMOS18	USER_SW3		6
A22	User switch	Input	LVCMOS18	USER_SW4		8
B22	User switch	Input	LVCMOS18	USER_SW5		10
A18	User switch	Input	LVCMOS18	USER_SW6		12
B18	User switch	Input	LVCMOS18	USER_SW7		–
A21	User switch	Input	LVCMOS18	USER_SW8		–

Figure 1-12 Shows the user test I/O connector J125.

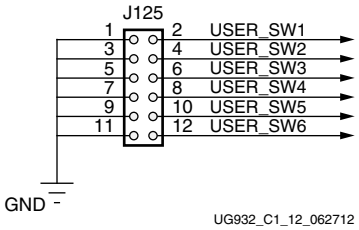

Figure 1-12: **User Test I/O**

User Push Buttons (Active High)

Callout 26, Figure 1-2.

SW4 and SW5 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-11. These switches can be used for any purpose.

Table 1-11: **User Push Buttons**

FPGA (U1)				Schematict Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
K18	User push button	Input	LVCMOS18	USER_PB1	SW5
G19	User push button	Input	LVCMOS18	USER_PB2	SW4

GTX Transceivers and Reference Clocks

Callout 27, Figure 1-2.

The KC724 board provides access to all GTX transceiver and reference clock pins on the FPGA as shown in Figure 1-13. The GTX transceivers are grouped into four sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: Figure 1-13 is for reference only and might not reflect the current revision of the board.

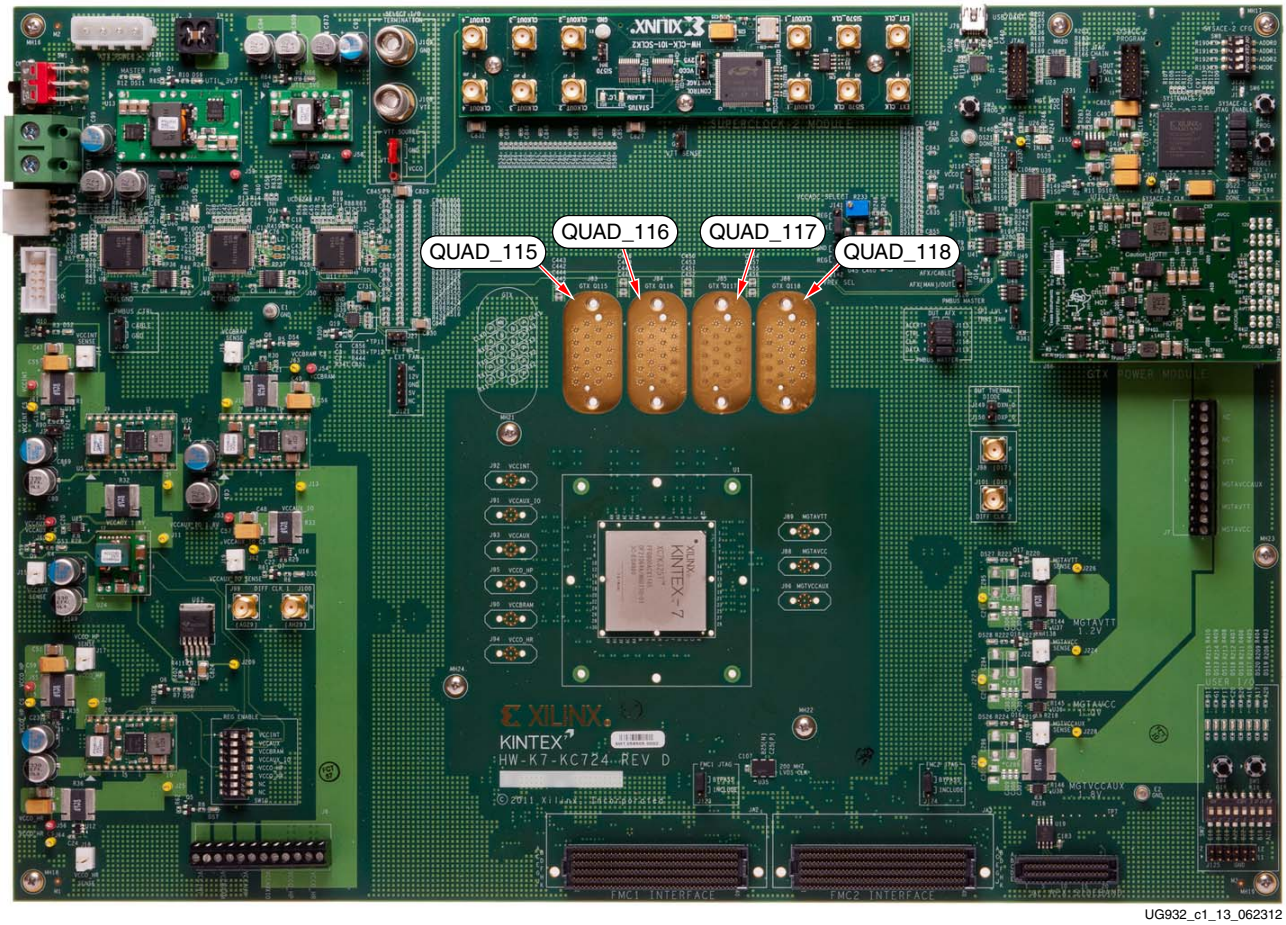

Figure 1-13: **GTX Quad Locations**

Each GTX Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about this or other cable assemblies. Figure 1-14 *A* shows the connector pad. Figure 1-14 *B* shows the connector pinout.

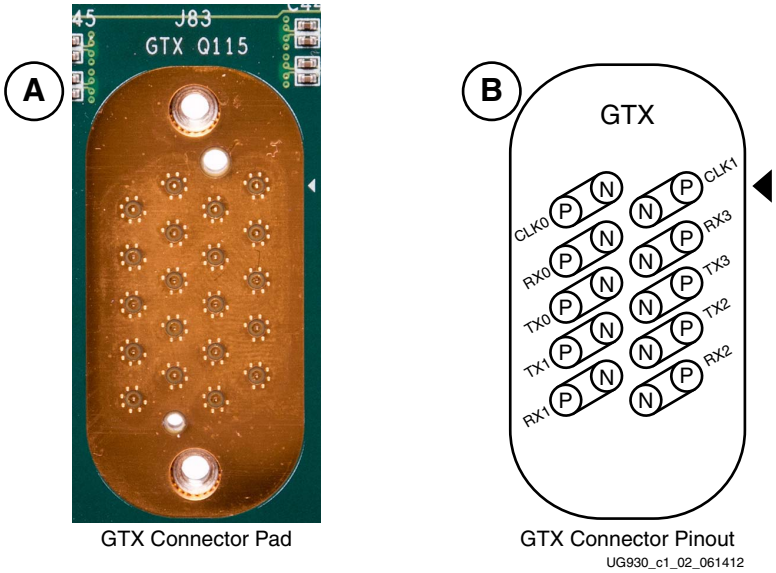

Figure 1-14: **A – GTX Connector Pad. B – GTX Connector Pinout**

Information for each GTX transceiver pin is shown in Table 1-12.

Table 1-12: **GTX Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
Y2	115_TX0_P	115	J83	2,805
Y1	115_TX0_N	115	J83	2,806
AA4	115_RX0_P	115	J83	2,898
AA3	115_RX0_N	115	J83	2,898
V2	115_TX1_P	115	J83	2,525
V1	115_TX1_N	115	J83	2,523
Y6	115_RX1_P	115	J83	2,489
Y5	115_RX1_N	115	J83	2,489
U4	115_TX2_P	115	J83	2,549
U3	115_TX2_N	115	J83	2,549
W4	115_RX2_P	115	J83	2,308
W3	115_RX2_N	115	J83	2,309
T2	115_TX3_P	115	J83	2,840
T1	115_TX3_N	115	J83	2,840

Table 1-12: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
V6	115_RX3_P	115	J83	2,933
V5	115_RX3_N	115	J83	2,933
P2	116_TX0_P	116	J84	2,677
P1	116_TX0_N	116	J84	2,677
T6	116_RX0_P	116	J84	2,667
T5	116_RX0_N	116	J84	2,668
N4	116_TX1_P	116	J84	2,469
N3	116_TX1_N	116	J84	2,469
R4	116_RX1_P	116	J84	2,207
R3	116_RX1_N	116	J84	2,207
M2	116_TX2_P	116	J84	2,359
M1	116_TX2_N	116	J84	2,357
P6	116_RX2_P	116	J84	2,218
P5	116_RX2_N	116	J84	2,218
L4	116_TX3_P	116	J84	2,555
L3	116_TX3_N	116	J84	2,555
M6	116_RX3_P	116	J84	2,821
M5	116_RX3_N	116	J84	2,821
K2	117_TX0_P	117	J85	2,617
K1	117_TX0_N	117	J85	2,616
K6	117_RX0_P	117	J85	2,886
K5	117_RX0_N	117	J85	2,886
J4	117_TX1_P	117	J85	2,400
J3	117_TX1_N	117	J85	2,401
H6	117_RX1_P	117	J85	2,337
H5	117_RX1_N	117	J85	2,337
H2	117_TX2_P	117	J85	2,635
H1	117_TX2_N	117	J85	2,634
G4	117_RX2_P	117	J85	2,349
G3	117_RX2_N	117	J85	2,349
F2	117_TX3_P	117	J85	2,823
F1	117_TX3_N	117	J85	2,823

Table 1-12: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
F6	117_RX3_P	117	J85	2,873
F5	117_RX3_N	117	J85	2,872
D2	118_TX0_P	118	J86	2,842
D1	118_TX0_N	118	J86	2,844
E4	118_RX0_P	118	J86	3,048
E3	118_RX0_N	118	J86	3,049
C4	118_TX1_P	118	J86	2,629
C3	118_TX1_N	118	J86	2,628
D6	118_RX1_P	118	J86	2,597
D5	118_RX1_N	118	J86	2,597
B2	118_TX2_P	118	J86	2,787
B1	118_TX2_N	118	J86	2,789
B6	118_RX2_P	118	J86	2,681
B5	118_RX2_N	118	J86	2,680
A4	118_TX3_P	118	J86	3,044
A3	118_TX3_N	118	J86	3,044
A8	118_RX3_P	118	J86	3,515
A7	118_RX3_N	118	J86	3,515

Information for each GTX transceiver clock input is shown in Table 1-13.

Table 1-13: **GTX Transceiver Clock Inputs to the FPGA**

U1 FPGA Pin	Net Name	Quad	Connector
R8	115_REFCLK0_P	115	J83
R7	115_REFCLK0_N	115	J83
U8	115_REFCLK1_P	115	J83
U7	115_REFCLK1_N	115	J83
L8	116_REFCLK0_P	116	J84
L7	116_REFCLK0_N	116	J84
N8	116_REFCLK1_P	116	J84
N7	116_REFCLK1_N	116	J84
G8	117_REFCLK0_P	117	J85
G7	117_REFCLK0_N	117	J85
J8	117_REFCLK1_P	117	J85

Table 1-13: **GTX Transceiver Clock Inputs to the FPGA *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector
J7	117_REFCLK1_N	117	J85
C8	118_REFCLK0_P	118	J86
C7	118_REFCLK0_N	118	J86
E8	118_REFCLK1_P	118	J86
E7	118_REFCLK1_N	118	J86

USB-to-UART Bridge

Callout 28, Figure 1-2.

Communications between the KC724 board and a host computer are through a USB cable connected to J79. Control is provided by U34, a USB-to-UART bridge (Silicon Laboratories CP2103). Table 1-14 lists the pin assignments and signals for the USB connector J79.

Table 1-14: **USB Mini-B Receptacle Pin Assignments and Signals**

J79 Pin	Signal Name	Description
1	VBUS	+5V into the CP2103 USB-to-UART bridge at U34. Used to sense USB network connection.
2	USB_DATA_N	Bidirectional differential serial data (N-side).
3	USB_DATA_P	Bidirectional differential serial data (P-side).
4	GROUND	Signal ground.

The CP2103 supports an I/O voltage range of 1.8V to 3.3V on the KC724 board. Xilinx UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U34 are listed in Table 1-15.

Table 1-15: **FPGA to UART Connections**

FPGA (U1)				Schematic Net Name	Device (U34)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
J18	RTS	Output	LVCMOS18	USB_CTS_I_B	22	CTS	Input
H20	CTS	Input	LVCMOS18	USB_RTS_0_B	23	RTS	Output
G20	TX	Output	LVCMOS18	USB_RXD_I	24	RXD	Input
J17	RX	Input	LVCMOS18	USB_TXD_0	25	TXD	Output

The bridge device also provides as many as 4 GPIO signals that can be defined for status and control information (Table 1-16).

Table 1-16: **CP2103 USB-to-UART Bridge User GPIO**

FPGA (U1)				Schematic Net Name	Device (U34)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
L17	SelectIO™	In/Out	LVCMOS18	USB_GPIO_0	19	GPIO	In/Out
H19	SelectIO	In/Out	LVCMOS18	USB_GPIO_1	18	GPIO	In/Out
J19	SelectIO	In/Out	LVCMOS18	USB_GPIO_2	17	GPIO	In/Out
H17	SelectIO	In/Out	LVCMOS18	USB_GPIO_3	16	GPIO	In/Out

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB-to-UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the KC724 board.

FPGA Mezzanine Card HPC Interface

Callout 29 and 30, Figure 1-2.

The KC724 board features two high pin count (HPC) connectors as defined by the VITA 57.1 FPGA Mezzanine card (FMC) specification. The FMC HPC connector is a 10 x 40 position socket. See Appendix C, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates.

FMC1 HPC connector provides connectivity for:

- 69 differential user defined pairs:
  - 34 LA pairs
  - 18 HA pairs
  - 17 HB pairs
- 2 differential clocks

FMC2 HPC connector JA3 provides connectivity for:

- 80 differential user defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 22 HB pairs
- 4 differential clocks

Note: The V_{ADJ} voltage for the FMC HPC connectors on the KC724 board tracks the I/O voltage of the FPGA banks that each FMC interface maps to. FMC1 tracks VCCO_HP. FMC2 tracks VCCO_HR.

The FMC HPC connectors on the KC724 board are identified as FMC1 at JA2 and FMC2 at JA3. The connections for each of these connectors are listed in Table 1-17 and Table 1-18, page 34 respectively.

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
AE10	FMC1_CLK0_M2C_P	H4
AF10	FMC1_CLK0_M2C_N	H5
AD18	FMC1_CLK1_M2C_P	G2
AE18	FMC1_CLK1_M2C_N	G3
AF17	FMC1_HA00_CC_P	F4
AG17	FMC1_HA00_CC_N	F5
AF18	FMC1_HA01_CC_P	E2
AG18	FMC1_HA01_CC_N	E3
AK16	FMC1_HA02_P	K7
AK15	FMC1_HA02_N	K8
AG15	FMC1_HA03_P	J6
AH15	FMC1_HA03_N	J7
AH16	FMC1_HA04_P	F7
AJ16	FMC1_HA04_N	F8
AF15	FMC1_HA05_P	E6
AG14	FMC1_HA05_N	E7
AH17	FMC1_HA06_P	K10
AJ17	FMC1_HA06_N	K11
AE16	FMC1_HA07_P	J9
AF16	FMC1_HA07_N	J10
AJ19	FMC1_HA08_P	F10
AK19	FMC1_HA08_N	F11
AG19	FMC1_HA09_P	E9
AH19	FMC1_HA09_N	E10
AJ18	FMC1_HA10_P	K13
AK18	FMC1_HA10_N	K14
AD19	FMC1_HA11_P	J12
AE19	FMC1_HA11_N	J13
AD17	FMC1_HA12_P	F13
AD16	FMC1_HA12_N	F14

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
Y19	FMC1_HA13_P	E12
Y18	FMC1_HA13_N	E13
AA18	FMC1_HA14_P	J15
AB18	FMC1_HA14_N	J16
AB19	FMC1_HA15_P	F16
AC19	FMC1_HA15_N	F17
AB17	FMC1_HA16_P	E15
AC17	FMC1_HA16_N	E16
AE15	FMC1_HA17_CC_P	K16
AE14	FMC1_HA17_CC_N	K17
AF6	FMC1_HB00_CC_P	K25
AG5	FMC1_HB00_CC_N	K26
AD4	FMC1_HB01_P	J24
AD3	FMC1_HB01_N	J25
AC2	FMC1_HB02_P	F22
AC1	FMC1_HB02_N	F23
AD2	FMC1_HB03_P	E21
AD1	FMC1_HB03_N	E22
AC5	FMC1_HB04_P	F25
AC4	FMC1_HB04_N	F26
AD6	FMC1_HB05_P	E24
AE6	FMC1_HB05_N	E25
AE5	FMC1_HB06_CC_P	K28
AF5	FMC1_HB06_CC_N	K29
AC7	FMC1_HB07_P	J27
AD7	FMC1_HB07_N	J28
AF3	FMC1_HB08_P	F28
AF2	FMC1_HB08_N	F29
AE1	FMC1_HB09_P	E27
AF1	FMC1_HB09_N	E28
AG4	FMC1_HB10_P	K31
AG3	FMC1_HB10_N	K32
AE4	FMC1_HB11_P	J30

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AE3	FMC1_HB11_N	J31
AH4	FMC1_HB12_P	F31
AJ4	FMC1_HB12_N	F32
AH6	FMC1_HB13_P	E30
AH5	FMC1_HB13_N	E31
AG2	FMC1_HB14_P	K34
AH1	FMC1_HB14_N	K35
AH2	FMC1_HB15_P	J33
AJ2	FMC1_HB15_N	J34
AJ1	FMC1_HB16_P	F34
AK1	FMC1_HB16_N	F35
U39.9(1)	FMC1_I2C_SCL	C30
U39.8(1)	FMC1_I2C_SDA	C31
AD12	FMC1_LA00_CC_P	G6
AD11	FMC1_LA00_CC_N	G7
AE11	FMC1_LA01_CC_P	D8
AF11	FMC1_LA01_CC_N	D9
AA12	FMC1_LA02_P	H7
AB12	FMC1_LA02_N	H8
AA8	FMC1_LA03_P	G9
AB8	FMC1_LA03_N	G10
AB9	FMC1_LA04_P	H10
AC9	FMC1_LA04_N	H11
Y11	FMC1_LA05_P	D11
Y10	FMC1_LA05_N	D12
AA11	FMC1_LA06_P	C10
AA10	FMC1_LA06_N	C11
AA13	FMC1_LA07_P	H13
AB13	FMC1_LA07_N	H14
AB10	FMC1_LA08_P	G12
AC10	FMC1_LA08_N	G13
AD8	FMC1_LA09_P	D14
AE8	FMC1_LA09_N	D15

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AC12	FMC1_LA10_P	C14
AC11	FMC1_LA10_N	C15
AD9	FMC1_LA11_P	H16
AE9	FMC1_LA11_N	H17
AJ9	FMC1_LA12_P	G15
AK9	FMC1_LA12_N	G16
AG9	FMC1_LA13_P	D17
AH9	FMC1_LA13_N	D18
AK11	FMC1_LA14_P	C18
AK10	FMC1_LA14_N	C19
AH11	FMC1_LA15_P	H19
AJ11	FMC1_LA15_N	H20
AE13	FMC1_LA16_P	G18
AF13	FMC1_LA16_N	G19
AG10	FMC1_LA17_CC_P	D20
AH10	FMC1_LA17_CC_N	D21
AK14	FMC1_LA18_CC_P	C22
AK13	FMC1_LA18_CC_N	C23
AH14	FMC1_LA19_P	H22
AJ14	FMC1_LA19_N	H23
AJ13	FMC1_LA20_P	G21
AJ12	FMC1_LA20_N	G22
AF12	FMC1_LA21_P	H25
AG12	FMC1_LA21_N	H26
AG13	FMC1_LA22_P	G24
AH12	FMC1_LA22_N	G25
AF8	FMC1_LA23_P	D23
AG8	FMC1_LA23_N	D24
AF7	FMC1_LA24_P	H28
AG7	FMC1_LA24_N	H29
AH7	FMC1_LA25_P	G27
AJ7	FMC1_LA25_N	G28
AJ6	FMC1_LA26_P	D26

Table 1-17: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AK6	FMC1_LA26_N	D27
AJ8	FMC1_LA27_P	C26
AK8	FMC1_LA27_N	C27
AK5	FMC1_LA28_P	H31
AK4	FMC1_LA28_N	H32
AA15	FMC1_LA29_P	G30
AB15	FMC1_LA29_N	G31
AC16	FMC1_LA30_P	H34
AC15	FMC1_LA30_N	H35
AC14	FMC1_LA31_P	G33
AD14	FMC1_LA31_N	G34
AA17	FMC1_LA32_P	H37
AA16	FMC1_LA32_N	H38
Y16	FMC1_LA33_P	G36
Y15	FMC1_LA33_N	G37
W19	FMC1_PRSNT_M2C_L	H2
U23.8(1)	FMC1_FMC2_TCK	D29
U23.3 / U19.1(1)	FMC1_TDI	D30
U23.6(1)	FMC1_FMC2_TMS	D33

Notes:

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U39.10 = U39 pin 10.

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
F12	FMC2_CLK0_M2C_P	H4
E13	FMC2_CLK0_M2C_N	H5
H14	FMC2_CLK1_M2C_P	G2
G14	FMC2_CLK1_M2C_N	G3
K28	FMC2_CLK2_BIDIR_P	K4
K29	FMC2_CLK2_BIDIR_N	K5
M28	FMC2_CLK3_BIDIR_P	J2
L28	FMC2_CLK3_BIDIR_N	J3
AD23	FMC2_HA00_CC_P	F4

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AE24	FMC2_HA00_CC_N	F5
AE23	FMC2_HA01_CC_P	E2
AF23	FMC2_HA01_CC_N	E3
AC20	FMC2_HA02_P	K7
AC21	FMC2_HA02_N	K8
AA20	FMC2_HA03_P	J6
AB20	FMC2_HA03_N	J7
AB24	FMC2_HA04_P	F7
AC25	FMC2_HA04_N	F8
AC22	FMC2_HA05_P	E6
AD22	FMC2_HA05_N	E7
AC24	FMC2_HA06_P	K10
AD24	FMC2_HA06_N	K11
AD21	FMC2_HA07_P	J9
AE21	FMC2_HA07_N	J10
AG24	FMC2_HA08_P	F10
AH24	FMC2_HA08_N	F11
AJ24	FMC2_HA09_P	E9
AK25	FMC2_HA09_N	E10
AE25	FMC2_HA10_P	K13
AF25	FMC2_HA10_N	K14
AK23	FMC2_HA11_P	J12
AK24	FMC2_HA11_N	J13
AG25	FMC2_HA12_P	F13
AH25	FMC2_HA12_N	F14
P24	FMC2_HA13_P	E12
R25	FMC2_HA13_N	E13
R20	FMC2_HA14_P	J15
R21	FMC2_HA14_N	J16
R23	FMC2_HA15_P	F16
R24	FMC2_HA15_N	F17
T20	FMC2_HA16_P	E15
T21	FMC2_HA16_N	E16

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AF22	FMC2_HA17_CC_P	K16
AG23	FMC2_HA17_CC_N	K17
T22	FMC2_HA18_P	J18
T23	FMC2_HA18_N	J19
W23	FMC2_HA19_P	F19
W24	FMC2_HA19_N	F20
U22	FMC2_HA20_P	E18
U23	FMC2_HA20_N	E19
V21	FMC2_HA21_P	K19
V22	FMC2_HA21_N	K20
U24	FMC2_HA22_P	J21
V24	FMC2_HA22_N	J22
W21	FMC2_HA23_P	K22
W22	FMC2_HA23_N	K23
G13	FMC2_HB00_CC_P	K25
F13	FMC2_HB00_CC_N	K26
L16	FMC2_HB01_P	J24
K16	FMC2_HB01_N	J25
L15	FMC2_HB02_P	F22
K15	FMC2_HB02_N	F23
L12	FMC2_HB03_P	E21
L13	FMC2_HB03_N	E22
K13	FMC2_HB04_P	F25
J13	FMC2_HB04_N	F26
K14	FMC2_HB05_P	E24
J14	FMC2_HB05_N	E25
J11	FMC2_HB06_CC_P	K28
J12	FMC2_HB06_CC_N	K29
L11	FMC2_HB07_P	J27
K11	FMC2_HB07_N	J28
H15	FMC2_HB08_P	F28
G15	FMC2_HB08_N	F29
J16	FMC2_HB09_P	E27

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
H16	FMC2_HB09_N	E28
H11	FMC2_HB10_P	K31
H12	FMC2_HB10_N	K32
A11	FMC2_HB11_P	J30
A12	FMC2_HB11_N	J31
D11	FMC2_HB12_P	F31
C11	FMC2_HB12_N	F32
F15	FMC2_HB13_P	E30
E16	FMC2_HB13_N	E31
E14	FMC2_HB14_P	K34
E15	FMC2_HB14_N	K35
D14	FMC2_HB15_P	J33
C14	FMC2_HB15_N	J34
B13	FMC2_HB16_P	F34
A13	FMC2_HB16_N	F35
D12	FMC2_HB17_CC_P	K37
D13	FMC2_HB17_CC_N	K38
C15	FMC2_HB18_P	J36
B15	FMC2_HB18_N	J37
B14	FMC2_HB19_P	E33
A15	FMC2_HB19_N	E34
M24	FMC2_HB20_P	F37
M25	FMC2_HB20_N	F38
M22	FMC2_HB21_P	E36
M23	FMC2_HB21_N	E37
U39.11(1)	FMC2_I2C_SCL	C30
U39.10(1)	FMC2_I2C_SDA	C31
L25	FMC2_LA00_CC_P	G6
K25	FMC2_LA00_CC_N	G7
L26	FMC2_LA01_CC_P	D8
L27	FMC2_LA01_CC_N	D9
J23	FMC2_LA02_P	H7
J24	FMC2_LA02_N	H8

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
L22	FMC2_LA03_P	G9
L23	FMC2_LA03_N	G10
K23	FMC2_LA04_P	H10
K24	FMC2_LA04_N	H11
L21	FMC2_LA05_P	D11
K21	FMC2_LA05_N	D12
J21	FMC2_LA06_P	C10
J22	FMC2_LA06_N	C11
M20	FMC2_LA07_P	H13
L20	FMC2_LA07_N	H14
J29	FMC2_LA08_P	G12
H29	FMC2_LA08_N	G13
J27	FMC2_LA09_P	D14
J28	FMC2_LA09_N	D15
L30	FMC2_LA10_P	C14
K30	FMC2_LA10_N	C15
K26	FMC2_LA11_P	H16
J26	FMC2_LA11_N	H17
M29	FMC2_LA12_P	G15
M30	FMC2_LA12_N	G16
N27	FMC2_LA13_P	D17
M27	FMC2_LA13_N	D18
N29	FMC2_LA14_P	C18
N30	FMC2_LA14_N	C19
N25	FMC2_LA15_P	H19
N26	FMC2_LA15_N	H20
N19	FMC2_LA16_P	G18
N20	FMC2_LA16_N	G19
U27	FMC2_LA17_CC_P	D20
U28	FMC2_LA17_CC_N	D21
T25	FMC2_LA18_CC_P	C22
U25	FMC2_LA18_CC_N	C23
N21	FMC2_LA19_P	H22

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
N22	FMC2_LA19_N	H23
P23	FMC2_LA20_P	G21
N24	FMC2_LA20_N	G22
P21	FMC2_LA21_P	H25
P22	FMC2_LA21_N	H26
U19	FMC2_LA22_P	G24
U20	FMC2_LA22_N	G25
P29	FMC2_LA23_P	D23
R29	FMC2_LA23_N	D24
P27	FMC2_LA24_P	H28
P28	FMC2_LA24_N	H29
R30	FMC2_LA25_P	G27
T30	FMC2_LA25_N	G28
P26	FMC2_LA26_P	D26
R26	FMC2_LA26_N	D27
R28	FMC2_LA27_P	C26
T28	FMC2_LA27_N	C27
T26	FMC2_LA28_P	H31
T27	FMC2_LA28_N	H32
U29	FMC2_LA29_P	G30
U30	FMC2_LA29_N	G31
V26	FMC2_LA30_P	H34
V27	FMC2_LA30_N	H35
V29	FMC2_LA31_P	G33
V30	FMC2_LA31_N	G34
V25	FMC2_LA32_P	H37
W26	FMC2_LA32_N	H38
V19	FMC2_LA33_P	G36
V20	FMC2_LA33_N	G37
F16	FMC2_PRSNT_M2C_L	H2
U23.8(1)	FMC1_FMC2_TCK	D29
U19.2 / U20.1(1)	FMC2_TDI	D30
U20.2 / U25.3(1)	FMC2_TDO	D31

Table 1-18: **VITA 57.1 FMC2 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
U23.6(1)	FMC1_FMC2_TMS	D33

Notes:

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U39.10 = U39 pin 10.

Table 1-19 lists the power supply voltages for the HPC connectors.

Table 1-19: **Power Supply Voltages for the HPC Connector**

Voltage Supply	Allowable Voltage Range		Number of Pins	I_{MAX} (Amps)	Tolerance	Maximum Capacitive Load
	FMC1	FMC2				
V_{ADJ}	VCCO_HP	VCCO_HR	4	4	±5%	1,000 µF
$3P3V_{AUX}$	3.3V		1	0.020	±5%	150 µF
3P3V	3.3V		4	3	±5%	1,000 µF
12P0V	12V		2	1	±5%	1,000 µF

XADC

Callout 31, Figure 1-2.

7 series FPGAs provide an analog front end (XADC) block. The XADC block includes a dual 12-bit, 1 MSPS analog-to-digital convertor (ADC) and on-chip sensors. See *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 2] for details on the capabilities of the analog front end.

The KC724 board supports the internal FPGA sensor measurement capabilities of the XADC. Internal measurements of the die temperature, VCCINT and VCCAUX can be monitored using the ChipScope™ Pro tool. The KC724 board provides two ways of setting the XADC reference voltage:

- **Jumper pins 1-2 (REG) on J142:** In this configuration, an onboard, low-temperature-coefficient 1.25V reference (U45, Texas Instruments part number REF3012AIDBZT) is connected to XADC VREFP.
- **Jumper pins 2-3 (AGND) on J142:** In this configuration, the FPGA's XADC uses an internal reference circuit.

Note: A jumper should be installed in one of the two positions during normal operation.

I2C Bus Management

Callout 32, Figure 1-2.

The I2C bus is controlled through U39, an 8-channel I2C-bus multiplexer (NXP Semiconductor PCA9547). The FPGA communicates with the multiplexer through I2C data and clock signals mapped to FPGA pins E21 and F21, respectively. The I2C idcode for the PCA9547 device is `0x70`. The bus hosts four components:

- SuperClock-2 module
- 7 series GTX transceiver power supply module
- FMC1
- FMC2

An I2C component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-20.

Table 1-20: **I2C Channel Assignments**

U39 Channel	I2C Component
0	SuperClock-2 module
1	7 series GTX transceiver power supply module
2	FMC1
3	FMC2

Appendix A

Default Jumper and Switch Positions

Table A-1 lists the jumpers that must be installed on the board for proper operation. These jumpers must be installed except where specifically noted in this user guide. PCB Assembly Drawing 0431643 shows the location and the default placement of all jumpers on their respective connectors on the board.

Note: Any jumper not listed in Table A-1 should be left open for normal operation.

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper	Comments
J48	<None>	Upper-left	CTRL (1–2)	UCD9248 reset pin
J49	<None>	Upper-left	CTRL (1–2)	UCD9248 reset pin
J50	<None>	Upper-left	CTRL (1–2)	UCD9248 reset pin
J4	UTIL_3V3	Upper-left	CTRL (1–2)	
J24	UTIL_5V0	Upper-left	CTRL (1–2)	
J78	VTT SOURCE	Upper-left	VTT → GND (1–2)	Red 20A jumper
J141	VCCADC SELECT	Upper-middle	VCCAUX (1–2)	
J142	VREF SEL	Upper-middle	REG (1–2)	
J140	PMBUS CTRL	Upper-right	ALWAYS ON (2-3)	

DIP switch SW10 enables the supply of onboard core power to the FPGA. For normal operation positions 1 through 6 must be set to the ON position as shown in Figure A-1.

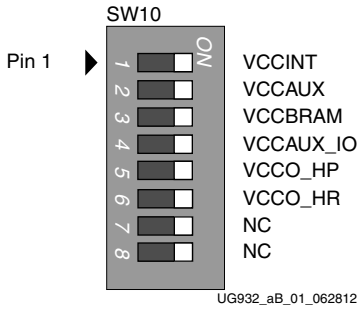

Figure A-1: **Default Switch Settings**

XILINX

Appendix B

Master Constraints File Listing

The KC724 board master Xilinx design constraints file (XDC) template provides for designs targeting the KC724 Kintex-7 FPGA GTX Transceiver Characterization Board. Net names in the constraints listed in this appendix correlate with net names on the KC724 board schematic. Identify the appropriate pins and replace the net names with the net names in the user RTL. See the *Vivado Design Suite User Guide, Using Contstraints* (UG903) [Ref 3] for more information.

The FMC connectors JA2 and JA3 are connected to VCCO_HP and VCCO_HR I/O banks, respectively. Because each FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Note: See the Kintex-7 FPGA KC724 Characterization Kit website for the latest release of the XDC file.

KC724 Board XDC Listing

```
#FMC1
set_property PACKAGE_PIN W19 [get_ports FMC1_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_PRSNT_M2C_L]
set_property PACKAGE_PIN AE10 [get_ports FMC1_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK0_M2C_P]
set_property PACKAGE_PIN AF10 [get_ports FMC1_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK0_M2C_N]
set_property PACKAGE_PIN AD18 [get_ports FMC1_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK1_M2C_P]
set_property PACKAGE_PIN AE18 [get_ports FMC1_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK1_M2C_N]
#FMC1 LA
set_property PACKAGE_PIN AD12 [get_ports FMC1_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA00_CC_P]
set_property PACKAGE_PIN AD11 [get_ports FMC1_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA00_CC_N]
set_property PACKAGE_PIN AE11 [get_ports FMC1_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA01_CC_P]
set_property PACKAGE_PIN AF11 [get_ports FMC1_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA01_CC_N]
set_property PACKAGE_PIN AA12 [get_ports FMC1_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA02_P]
set_property PACKAGE_PIN AB12 [get_ports FMC1_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA02_N]
set_property PACKAGE_PIN AA8 [get_ports FMC1_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA03_P]
set_property PACKAGE_PIN AB8 [get_ports FMC1_LA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA03_N]
set_property PACKAGE_PIN AB9 [get_ports FMC1_LA04_P]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA04_P]
set_property PACKAGE_PIN AC9 [get_ports FMC1_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA04_N]
set_property PACKAGE_PIN Y11 [get_ports FMC1_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA05_P]
set_property PACKAGE_PIN Y10 [get_ports FMC1_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA05_N]
set_property PACKAGE_PIN AA11 [get_ports FMC1_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA06_P]
set_property PACKAGE_PIN AA10 [get_ports FMC1_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA06_N]
set_property PACKAGE_PIN AA13 [get_ports FMC1_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA07_P]
set_property PACKAGE_PIN AB13 [get_ports FMC1_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA07_N]
set_property PACKAGE_PIN AB10 [get_ports FMC1_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA08_P]
set_property PACKAGE_PIN AC10 [get_ports FMC1_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA08_N]
set_property PACKAGE_PIN AD8 [get_ports FMC1_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA09_P]
set_property PACKAGE_PIN AE8 [get_ports FMC1_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA09_N]
set_property PACKAGE_PIN AC12 [get_ports FMC1_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA10_P]
set_property PACKAGE_PIN AC11 [get_ports FMC1_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA10_N]
set_property PACKAGE_PIN AD9 [get_ports FMC1_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA11_P]
set_property PACKAGE_PIN AE9 [get_ports FMC1_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA11_N]
set_property PACKAGE_PIN AJ9 [get_ports FMC1_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA12_P]
set_property PACKAGE_PIN AK9 [get_ports FMC1_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA12_N]
set_property PACKAGE_PIN AG9 [get_ports FMC1_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA13_P]
set_property PACKAGE_PIN AH9 [get_ports FMC1_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA13_N]
set_property PACKAGE_PIN AK11 [get_ports FMC1_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA14_P]
set_property PACKAGE_PIN AK10 [get_ports FMC1_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA14_N]
set_property PACKAGE_PIN AH11 [get_ports FMC1_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA15_P]
set_property PACKAGE_PIN AJ11 [get_ports FMC1_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA15_N]
set_property PACKAGE_PIN AE13 [get_ports FMC1_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA16_P]
set_property PACKAGE_PIN AF13 [get_ports FMC1_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA16_N]
set_property PACKAGE_PIN AG10 [get_ports FMC1_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA17_CC_P]
set_property PACKAGE_PIN AH10 [get_ports FMC1_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA17_CC_N]
set_property PACKAGE_PIN AK14 [get_ports FMC1_LA18_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA18_CC_P]
set_property PACKAGE_PIN AK13 [get_ports FMC1_LA18_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA18_CC_N]
```

```
set_property PACKAGE_PIN AH14 [get_ports FMC1_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA19_P]
set_property PACKAGE_PIN AJ14 [get_ports FMC1_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA19_N]
set_property PACKAGE_PIN AJ13 [get_ports FMC1_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA20_P]
set_property PACKAGE_PIN AJ12 [get_ports FMC1_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA20_N]
set_property PACKAGE_PIN AF12 [get_ports FMC1_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA21_P]
set_property PACKAGE_PIN AG12 [get_ports FMC1_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA21_N]
set_property PACKAGE_PIN AG13 [get_ports FMC1_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA22_P]
set_property PACKAGE_PIN AH12 [get_ports FMC1_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA22_N]
set_property PACKAGE_PIN AF8 [get_ports FMC1_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA23_P]
set_property PACKAGE_PIN AG8 [get_ports FMC1_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA23_N]
set_property PACKAGE_PIN AF7 [get_ports FMC1_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA24_P]
set_property PACKAGE_PIN AG7 [get_ports FMC1_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA24_N]
set_property PACKAGE_PIN AH7 [get_ports FMC1_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA25_P]
set_property PACKAGE_PIN AJ7 [get_ports FMC1_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA25_N]
set_property PACKAGE_PIN AJ6 [get_ports FMC1_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA26_P]
set_property PACKAGE_PIN AK6 [get_ports FMC1_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA26_N]
set_property PACKAGE_PIN AJ8 [get_ports FMC1_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA27_P]
set_property PACKAGE_PIN AK8 [get_ports FMC1_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA27_N]
set_property PACKAGE_PIN AK5 [get_ports FMC1_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA28_P]
set_property PACKAGE_PIN AK4 [get_ports FMC1_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA28_N]
set_property PACKAGE_PIN AA15 [get_ports FMC1_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA29_P]
set_property PACKAGE_PIN AB15 [get_ports FMC1_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA29_N]
set_property PACKAGE_PIN AC16 [get_ports FMC1_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA30_P]
set_property PACKAGE_PIN AC15 [get_ports FMC1_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA30_N]
set_property PACKAGE_PIN AC14 [get_ports FMC1_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA31_P]
set_property PACKAGE_PIN AD14 [get_ports FMC1_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA31_N]
set_property PACKAGE_PIN AA17 [get_ports FMC1_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA32_P]
set_property PACKAGE_PIN AA16 [get_ports FMC1_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA32_N]
set_property PACKAGE_PIN Y16 [get_ports FMC1_LA33_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA33_P]
set_property PACKAGE_PIN Y15 [get_ports FMC1_LA33_N]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA33_N]
#FMC1 HA
set_property PACKAGE_PIN AF17 [get_ports FMC1_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA00_CC_P]
set_property PACKAGE_PIN AG17 [get_ports FMC1_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA00_CC_N]
set_property PACKAGE_PIN AF18 [get_ports FMC1_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA01_CC_P]
set_property PACKAGE_PIN AG18 [get_ports FMC1_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA01_CC_N]
set_property PACKAGE_PIN AK16 [get_ports FMC1_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA02_P]
set_property PACKAGE_PIN AK15 [get_ports FMC1_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA02_N]
set_property PACKAGE_PIN AG15 [get_ports FMC1_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA03_P]
set_property PACKAGE_PIN AH15 [get_ports FMC1_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA03_N]
set_property PACKAGE_PIN AH16 [get_ports FMC1_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA04_P]
set_property PACKAGE_PIN AJ16 [get_ports FMC1_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA04_N]
set_property PACKAGE_PIN AF15 [get_ports FMC1_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA05_P]
set_property PACKAGE_PIN AG14 [get_ports FMC1_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA05_N]
set_property PACKAGE_PIN AH17 [get_ports FMC1_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA06_P]
set_property PACKAGE_PIN AJ17 [get_ports FMC1_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA06_N]
set_property PACKAGE_PIN AE16 [get_ports FMC1_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA07_P]
set_property PACKAGE_PIN AF16 [get_ports FMC1_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA07_N]
set_property PACKAGE_PIN AJ19 [get_ports FMC1_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA08_P]
set_property PACKAGE_PIN AK19 [get_ports FMC1_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA08_N]
set_property PACKAGE_PIN AG19 [get_ports FMC1_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA09_P]
set_property PACKAGE_PIN AH19 [get_ports FMC1_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA09_N]
set_property PACKAGE_PIN AJ18 [get_ports FMC1_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA10_P]
set_property PACKAGE_PIN AK18 [get_ports FMC1_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA10_N]
set_property PACKAGE_PIN AD19 [get_ports FMC1_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA11_P]
set_property PACKAGE_PIN AE19 [get_ports FMC1_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA11_N]
set_property PACKAGE_PIN AD17 [get_ports FMC1_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA12_P]
set_property PACKAGE_PIN AD16 [get_ports FMC1_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA12_N]
set_property PACKAGE_PIN Y19 [get_ports FMC1_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA13_P]
set_property PACKAGE_PIN Y18 [get_ports FMC1_HA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA13_N]
set_property PACKAGE_PIN AA18 [get_ports FMC1_HA14_P]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA14_P]
set_property PACKAGE_PIN AB18 [get_ports FMC1_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA14_N]
set_property PACKAGE_PIN AB19 [get_ports FMC1_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA15_P]
set_property PACKAGE_PIN AC19 [get_ports FMC1_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA15_N]
set_property PACKAGE_PIN AB17 [get_ports FMC1_HA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA16_P]
set_property PACKAGE_PIN AC17 [get_ports FMC1_HA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA16_N]
set_property PACKAGE_PIN AE15 [get_ports FMC1_HA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA17_CC_P]
set_property PACKAGE_PIN AE14 [get_ports FMC1_HA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA17_CC_N]
#FMC1 HB
set_property PACKAGE_PIN AF6 [get_ports FMC1_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB00_CC_P]
set_property PACKAGE_PIN AG5 [get_ports FMC1_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB00_CC_N]
set_property PACKAGE_PIN AD4 [get_ports FMC1_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB01_P]
set_property PACKAGE_PIN AD3 [get_ports FMC1_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB01_N]
set_property PACKAGE_PIN AC2 [get_ports FMC1_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB02_P]
set_property PACKAGE_PIN AC1 [get_ports FMC1_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB02_N]
set_property PACKAGE_PIN AD2 [get_ports FMC1_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB03_P]
set_property PACKAGE_PIN AD1 [get_ports FMC1_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB03_N]
set_property PACKAGE_PIN AC5 [get_ports FMC1_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB04_P]
set_property PACKAGE_PIN AC4 [get_ports FMC1_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB04_N]
set_property PACKAGE_PIN AD6 [get_ports FMC1_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB05_P]
set_property PACKAGE_PIN AE6 [get_ports FMC1_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB05_N]
set_property PACKAGE_PIN AE5 [get_ports FMC1_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB06_CC_P]
set_property PACKAGE_PIN AF5 [get_ports FMC1_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB06_CC_N]
set_property PACKAGE_PIN AC7 [get_ports FMC1_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB07_P]
set_property PACKAGE_PIN AD7 [get_ports FMC1_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB07_N]
set_property PACKAGE_PIN AF3 [get_ports FMC1_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB08_P]
set_property PACKAGE_PIN AF2 [get_ports FMC1_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB08_N]
set_property PACKAGE_PIN AE1 [get_ports FMC1_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB09_P]
set_property PACKAGE_PIN AF1 [get_ports FMC1_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB09_N]
set_property PACKAGE_PIN AG4 [get_ports FMC1_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB10_P]
set_property PACKAGE_PIN AG3 [get_ports FMC1_HB10_N]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB10_N]
set_property PACKAGE_PIN AE4 [get_ports FMC1_HB11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB11_P]
set_property PACKAGE_PIN AE3 [get_ports FMC1_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB11_N]
set_property PACKAGE_PIN AH4 [get_ports FMC1_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB12_P]
set_property PACKAGE_PIN AJ4 [get_ports FMC1_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB12_N]
set_property PACKAGE_PIN AH6 [get_ports FMC1_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB13_P]
set_property PACKAGE_PIN AH5 [get_ports FMC1_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB13_N]
set_property PACKAGE_PIN AG2 [get_ports FMC1_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB14_P]
set_property PACKAGE_PIN AH1 [get_ports FMC1_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB14_N]
set_property PACKAGE_PIN AH2 [get_ports FMC1_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB15_P]
set_property PACKAGE_PIN AJ2 [get_ports FMC1_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB15_N]
set_property PACKAGE_PIN AJ1 [get_ports FMC1_HB16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB16_P]
set_property PACKAGE_PIN AK1 [get_ports FMC1_HB16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB16_N]
#FMC2
set_property PACKAGE_PIN F16 [get_ports FMC2_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_PRSNT_M2C_L]
set_property PACKAGE_PIN F12 [get_ports FMC2_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK0_M2C_P]
set_property PACKAGE_PIN E13 [get_ports FMC2_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK0_M2C_N]
set_property PACKAGE_PIN H14 [get_ports FMC2_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK1_M2C_P]
set_property PACKAGE_PIN G14 [get_ports FMC2_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK1_M2C_N]
set_property PACKAGE_PIN K28 [get_ports FMC2_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK2_BIDIR_P]
set_property PACKAGE_PIN K29 [get_ports FMC2_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK2_BIDIR_N]
set_property PACKAGE_PIN M28 [get_ports FMC2_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK3_BIDIR_P]
set_property PACKAGE_PIN L28 [get_ports FMC2_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK3_BIDIR_N]
#FMC2 LA
set_property PACKAGE_PIN L25 [get_ports FMC2_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA00_CC_P]
set_property PACKAGE_PIN K25 [get_ports FMC2_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA00_CC_N]
set_property PACKAGE_PIN L26 [get_ports FMC2_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA01_CC_P]
set_property PACKAGE_PIN L27 [get_ports FMC2_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA01_CC_N]
set_property PACKAGE_PIN J23 [get_ports FMC2_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA02_P]
set_property PACKAGE_PIN J24 [get_ports FMC2_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA02_N]
set_property PACKAGE_PIN L22 [get_ports FMC2_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA03_P]
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set_property PACKAGE_PIN L23 [get_ports FMC2_LA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA03_N]
set_property PACKAGE_PIN K23 [get_ports FMC2_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA04_P]
set_property PACKAGE_PIN K24 [get_ports FMC2_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA04_N]
set_property PACKAGE_PIN L21 [get_ports FMC2_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA05_P]
set_property PACKAGE_PIN K21 [get_ports FMC2_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA05_N]
set_property PACKAGE_PIN J21 [get_ports FMC2_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA06_P]
set_property PACKAGE_PIN J22 [get_ports FMC2_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA06_N]
set_property PACKAGE_PIN M20 [get_ports FMC2_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA07_P]
set_property PACKAGE_PIN L20 [get_ports FMC2_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA07_N]
set_property PACKAGE_PIN J29 [get_ports FMC2_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA08_P]
set_property PACKAGE_PIN H29 [get_ports FMC2_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA08_N]
set_property PACKAGE_PIN J27 [get_ports FMC2_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA09_P]
set_property PACKAGE_PIN J28 [get_ports FMC2_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA09_N]
set_property PACKAGE_PIN L30 [get_ports FMC2_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA10_P]
set_property PACKAGE_PIN K30 [get_ports FMC2_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA10_N]
set_property PACKAGE_PIN K26 [get_ports FMC2_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA11_P]
set_property PACKAGE_PIN J26 [get_ports FMC2_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA11_N]
set_property PACKAGE_PIN M29 [get_ports FMC2_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA12_P]
set_property PACKAGE_PIN M30 [get_ports FMC2_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA12_N]
set_property PACKAGE_PIN N27 [get_ports FMC2_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA13_P]
set_property PACKAGE_PIN M27 [get_ports FMC2_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA13_N]
set_property PACKAGE_PIN N29 [get_ports FMC2_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA14_P]
set_property PACKAGE_PIN N30 [get_ports FMC2_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA14_N]
set_property PACKAGE_PIN N25 [get_ports FMC2_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA15_P]
set_property PACKAGE_PIN N26 [get_ports FMC2_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA15_N]
set_property PACKAGE_PIN N19 [get_ports FMC2_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA16_P]
set_property PACKAGE_PIN N20 [get_ports FMC2_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA16_N]
set_property PACKAGE_PIN U27 [get_ports FMC2_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA17_CC_P]
set_property PACKAGE_PIN U28 [get_ports FMC2_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA17_CC_N]
set_property PACKAGE_PIN T25 [get_ports FMC2_LA18_CC_P]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA18_CC_P]
set_property PACKAGE_PIN U25 [get_ports FMC2_LA18_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA18_CC_N]
set_property PACKAGE_PIN N21 [get_ports FMC2_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA19_P]
set_property PACKAGE_PIN N22 [get_ports FMC2_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA19_N]
set_property PACKAGE_PIN P23 [get_ports FMC2_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA20_P]
set_property PACKAGE_PIN N24 [get_ports FMC2_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA20_N]
set_property PACKAGE_PIN P21 [get_ports FMC2_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA21_P]
set_property PACKAGE_PIN P22 [get_ports FMC2_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA21_N]
set_property PACKAGE_PIN U19 [get_ports FMC2_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA22_P]
set_property PACKAGE_PIN U20 [get_ports FMC2_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA22_N]
set_property PACKAGE_PIN P29 [get_ports FMC2_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA23_P]
set_property PACKAGE_PIN R29 [get_ports FMC2_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA23_N]
set_property PACKAGE_PIN P27 [get_ports FMC2_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA24_P]
set_property PACKAGE_PIN P28 [get_ports FMC2_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA24_N]
set_property PACKAGE_PIN R30 [get_ports FMC2_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA25_P]
set_property PACKAGE_PIN T30 [get_ports FMC2_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA25_N]
set_property PACKAGE_PIN P26 [get_ports FMC2_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA26_P]
set_property PACKAGE_PIN R26 [get_ports FMC2_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA26_N]
set_property PACKAGE_PIN R28 [get_ports FMC2_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA27_P]
set_property PACKAGE_PIN T28 [get_ports FMC2_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA27_N]
set_property PACKAGE_PIN T26 [get_ports FMC2_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA28_P]
set_property PACKAGE_PIN T27 [get_ports FMC2_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA28_N]
set_property PACKAGE_PIN U29 [get_ports FMC2_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA29_P]
set_property PACKAGE_PIN U30 [get_ports FMC2_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA29_N]
set_property PACKAGE_PIN V26 [get_ports FMC2_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA30_P]
set_property PACKAGE_PIN V27 [get_ports FMC2_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA30_N]
set_property PACKAGE_PIN V29 [get_ports FMC2_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA31_P]
set_property PACKAGE_PIN V30 [get_ports FMC2_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA31_N]
set_property PACKAGE_PIN V25 [get_ports FMC2_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA32_P]
set_property PACKAGE_PIN W26 [get_ports FMC2_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA32_N]
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set_property PACKAGE_PIN V19 [get_ports FMC2_LA33_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA33_P]
set_property PACKAGE_PIN V20 [get_ports FMC2_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA33_N]
set_property PACKAGE_PIN AD23 [get_ports FMC2_HA00_CC_P]
#FMC2 HA
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA00_CC_P]
set_property PACKAGE_PIN AE24 [get_ports FMC2_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA00_CC_N]
set_property PACKAGE_PIN AE23 [get_ports FMC2_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA01_CC_P]
set_property PACKAGE_PIN AF23 [get_ports FMC2_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA01_CC_N]
set_property PACKAGE_PIN AC20 [get_ports FMC2_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA02_P]
set_property PACKAGE_PIN AC21 [get_ports FMC2_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA02_N]
set_property PACKAGE_PIN AA20 [get_ports FMC2_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA03_P]
set_property PACKAGE_PIN AB20 [get_ports FMC2_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA03_N]
set_property PACKAGE_PIN AB24 [get_ports FMC2_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA04_P]
set_property PACKAGE_PIN AC25 [get_ports FMC2_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA04_N]
set_property PACKAGE_PIN AC22 [get_ports FMC2_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA05_P]
set_property PACKAGE_PIN AD22 [get_ports FMC2_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA05_N]
set_property PACKAGE_PIN AC24 [get_ports FMC2_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA06_P]
set_property PACKAGE_PIN AD24 [get_ports FMC2_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA06_N]
set_property PACKAGE_PIN AD21 [get_ports FMC2_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA07_P]
set_property PACKAGE_PIN AE21 [get_ports FMC2_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA07_N]
set_property PACKAGE_PIN AG24 [get_ports FMC2_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA08_P]
set_property PACKAGE_PIN AH24 [get_ports FMC2_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA08_N]
set_property PACKAGE_PIN AJ24 [get_ports FMC2_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA09_P]
set_property PACKAGE_PIN AK25 [get_ports FMC2_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA09_N]
set_property PACKAGE_PIN AE25 [get_ports FMC2_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA10_P]
set_property PACKAGE_PIN AF25 [get_ports FMC2_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA10_N]
set_property PACKAGE_PIN AK23 [get_ports FMC2_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA11_P]
set_property PACKAGE_PIN AK24 [get_ports FMC2_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA11_N]
set_property PACKAGE_PIN AG25 [get_ports FMC2_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA12_P]
set_property PACKAGE_PIN AH25 [get_ports FMC2_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA12_N]
set_property PACKAGE_PIN P24 [get_ports FMC2_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA13_P]
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set_property PACKAGE_PIN R25 [get_ports FMC2_HA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA13_N]
set_property PACKAGE_PIN R20 [get_ports FMC2_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA14_P]
set_property PACKAGE_PIN R21 [get_ports FMC2_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA14_N]
set_property PACKAGE_PIN R23 [get_ports FMC2_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA15_P]
set_property PACKAGE_PIN R24 [get_ports FMC2_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA15_N]
set_property PACKAGE_PIN T20 [get_ports FMC2_HA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA16_P]
set_property PACKAGE_PIN T21 [get_ports FMC2_HA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA16_N]
set_property PACKAGE_PIN AF22 [get_ports FMC2_HA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA17_CC_P]
set_property PACKAGE_PIN AG23 [get_ports FMC2_HA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA17_CC_N]
set_property PACKAGE_PIN T22 [get_ports FMC2_HA18_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA18_P]
set_property PACKAGE_PIN T23 [get_ports FMC2_HA18_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA18_N]
set_property PACKAGE_PIN W23 [get_ports FMC2_HA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA19_P]
set_property PACKAGE_PIN W24 [get_ports FMC2_HA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA19_N]
set_property PACKAGE_PIN U22 [get_ports FMC2_HA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA20_P]
set_property PACKAGE_PIN U23 [get_ports FMC2_HA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA20_N]
set_property PACKAGE_PIN V21 [get_ports FMC2_HA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA21_P]
set_property PACKAGE_PIN V22 [get_ports FMC2_HA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA21_N]
set_property PACKAGE_PIN U24 [get_ports FMC2_HA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA22_P]
set_property PACKAGE_PIN V24 [get_ports FMC2_HA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA22_N]
set_property PACKAGE_PIN W21 [get_ports FMC2_HA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA23_P]
set_property PACKAGE_PIN W22 [get_ports FMC2_HA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA23_N]
#FMC2 HB
set_property PACKAGE_PIN G13 [get_ports FMC2_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB00_CC_P]
set_property PACKAGE_PIN F13 [get_ports FMC2_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB00_CC_N]
set_property PACKAGE_PIN L16 [get_ports FMC2_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB01_P]
set_property PACKAGE_PIN K16 [get_ports FMC2_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB01_N]
set_property PACKAGE_PIN L15 [get_ports FMC2_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB02_P]
set_property PACKAGE_PIN K15 [get_ports FMC2_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB02_N]
set_property PACKAGE_PIN L12 [get_ports FMC2_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB03_P]
set_property PACKAGE_PIN L13 [get_ports FMC2_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB03_N]
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set_property PACKAGE_PIN K13 [get_ports FMC2_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB04_P]
set_property PACKAGE_PIN J13 [get_ports FMC2_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB04_N]
set_property PACKAGE_PIN K14 [get_ports FMC2_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB05_P]
set_property PACKAGE_PIN J14 [get_ports FMC2_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB05_N]
set_property PACKAGE_PIN J11 [get_ports FMC2_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB06_CC_P]
set_property PACKAGE_PIN J12 [get_ports FMC2_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB06_CC_N]
set_property PACKAGE_PIN L11 [get_ports FMC2_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB07_P]
set_property PACKAGE_PIN K11 [get_ports FMC2_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB07_N]
set_property PACKAGE_PIN H15 [get_ports FMC2_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB08_P]
set_property PACKAGE_PIN G15 [get_ports FMC2_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB08_N]
set_property PACKAGE_PIN J16 [get_ports FMC2_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB09_P]
set_property PACKAGE_PIN H16 [get_ports FMC2_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB09_N]
set_property PACKAGE_PIN H11 [get_ports FMC2_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB10_P]
set_property PACKAGE_PIN H12 [get_ports FMC2_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB10_N]
set_property PACKAGE_PIN A11 [get_ports FMC2_HB11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB11_P]
set_property PACKAGE_PIN A12 [get_ports FMC2_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB11_N]
set_property PACKAGE_PIN D11 [get_ports FMC2_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB12_P]
set_property PACKAGE_PIN C11 [get_ports FMC2_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB12_N]
set_property PACKAGE_PIN F15 [get_ports FMC2_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB13_P]
set_property PACKAGE_PIN E16 [get_ports FMC2_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB13_N]
set_property PACKAGE_PIN E14 [get_ports FMC2_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB14_P]
set_property PACKAGE_PIN E15 [get_ports FMC2_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB14_N]
set_property PACKAGE_PIN D14 [get_ports FMC2_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB15_P]
set_property PACKAGE_PIN C14 [get_ports FMC2_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB15_N]
set_property PACKAGE_PIN B13 [get_ports FMC2_HB16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB16_P]
set_property PACKAGE_PIN A13 [get_ports FMC2_HB16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB16_N]
set_property PACKAGE_PIN D12 [get_ports FMC2_HB17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB17_CC_P]
set_property PACKAGE_PIN D13 [get_ports FMC2_HB17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB17_CC_N]
set_property PACKAGE_PIN C15 [get_ports FMC2_HB18_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB18_P]
set_property PACKAGE_PIN B15 [get_ports FMC2_HB18_N]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB18_N]
set_property PACKAGE_PIN B14 [get_ports FMC2_HB19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB19_P]
set_property PACKAGE_PIN A15 [get_ports FMC2_HB19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB19_N]
set_property PACKAGE_PIN M24 [get_ports FMC2_HB20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB20_P]
set_property PACKAGE_PIN M25 [get_ports FMC2_HB20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB20_N]
set_property PACKAGE_PIN M22 [get_ports FMC2_HB21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB21_P]
set_property PACKAGE_PIN M23 [get_ports FMC2_HB21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB21_N]
#SuperClock2_MODULE
set_property PACKAGE_PIN B24 [get_ports CM_RST]
set_property IOSTANDARD LVCMOS18 [get_ports CM_RST]
set_property PACKAGE_PIN G30 [get_ports CM_CTRL_0]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_0]
set_property PACKAGE_PIN H30 [get_ports CM_CTRL_1]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_1]
set_property PACKAGE_PIN H27 [get_ports CM_CTRL_2]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_2]
set_property PACKAGE_PIN H26 [get_ports CM_CTRL_3]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_3]
set_property PACKAGE_PIN F30 [get_ports CM_CTRL_4]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_4]
set_property PACKAGE_PIN G29 [get_ports CM_CTRL_5]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_5]
set_property PACKAGE_PIN F27 [get_ports CM_CTRL_6]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_6]
set_property PACKAGE_PIN G27 [get_ports CM_CTRL_7]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_7]
set_property PACKAGE_PIN F28 [get_ports CM_CTRL_8]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_8]
set_property PACKAGE_PIN G28 [get_ports CM_CTRL_9]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_9]
set_property PACKAGE_PIN H25 [get_ports CM_CTRL_10]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_10]
set_property PACKAGE_PIN H24 [get_ports CM_CTRL_11]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_11]
set_property PACKAGE_PIN E30 [get_ports CM_CTRL_12]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_12]
set_property PACKAGE_PIN E29 [get_ports CM_CTRL_13]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_13]
set_property PACKAGE_PIN A30 [get_ports CM_CTRL_14]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_14]
set_property PACKAGE_PIN B30 [get_ports CM_CTRL_15]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_15]
set_property PACKAGE_PIN C30 [get_ports CM_CTRL_16]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_16]
set_property PACKAGE_PIN D29 [get_ports CM_CTRL_17]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_17]
set_property PACKAGE_PIN B29 [get_ports CM_CTRL_18]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_18]
set_property PACKAGE_PIN C29 [get_ports CM_CTRL_19]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_19]
set_property PACKAGE_PIN A26 [get_ports CM_CTRL_20]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_20]
set_property PACKAGE_PIN A25 [get_ports CM_CTRL_21]
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set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_21]
set_property PACKAGE_PIN A28 [get_ports CM_CTRL_22]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_22]
set_property PACKAGE_PIN B28 [get_ports CM_CTRL_23]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_23]
set_property PACKAGE_PIN F11 [get_ports CM_LVDS1_P]
set_property IOSTANDARD LVDS_25 [get_ports CM_LVDS1_P]
set_property PACKAGE_PIN E11 [get_ports CM_LVDS1_N]
set_property IOSTANDARD LVDS_25 [get_ports CM_LVDS1_N]
set_property PACKAGE_PIN C12 [get_ports CM_LVDS2_P]
set_property IOSTANDARD LVDS_25 [get_ports CM_LVDS2_P]
set_property PACKAGE_PIN B12 [get_ports CM_LVDS2_N]
set_property IOSTANDARD LVDS_25 [get_ports CM_LVDS2_N]
set_property PACKAGE_PIN AJ3 [get_ports CM_LVDS3_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS3_P]
set_property PACKAGE_PIN AK3 [get_ports CM_LVDS3_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS3_N]
set_property PACKAGE_PIN D26 [get_ports CM_GCLK_P]
set_property IOSTANDARD LVDS_25 [get_ports CM_GCLK_P]
set_property PACKAGE_PIN C26 [get_ports CM_GCLK_N]
set_property IOSTANDARD LVDS_25 [get_ports CM_GCLK_N]
#SWITCHES
set_property PACKAGE_PIN E18 [get_ports USER_SW1]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW1]
set_property PACKAGE_PIN B19 [get_ports USER_SW2]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW2]
set_property PACKAGE_PIN C19 [get_ports USER_SW3]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW3]
set_property PACKAGE_PIN A22 [get_ports USER_SW4]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW4]
set_property PACKAGE_PIN B22 [get_ports USER_SW5]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW5]
set_property PACKAGE_PIN A18 [get_ports USER_SW6]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW6]
set_property PACKAGE_PIN B18 [get_ports USER_SW7]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW7]
set_property PACKAGE_PIN A21 [get_ports USER_SW8]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW8]
#BUTTONS
set_property PACKAGE_PIN K18 [get_ports USER_PB1]
set_property IOSTANDARD LVCMOS18 [get_ports USER_PB1]
set_property PACKAGE_PIN G19 [get_ports USER_PB2]
set_property IOSTANDARD LVCMOS18 [get_ports USER_PB2]
#SMAs
set_property PACKAGE_PIN AG29 [get_ports CLK_DIFF_1_P]
set_property IOSTANDARD LVDS_25 [get_ports CLK_DIFF_1_P]
set_property PACKAGE_PIN AH29 [get_ports CLK_DIFF_1_N]
set_property IOSTANDARD LVDS_25 [get_ports CLK_DIFF_1_N]
set_property PACKAGE_PIN D17 [get_ports CLK_DIFF_2_P]
set_property IOSTANDARD LVDS_25 [get_ports CLK_DIFF_2_P]
set_property PACKAGE_PIN D18 [get_ports CLK_DIFF_2_N]
set_property IOSTANDARD LVDS_25 [get_ports CLK_DIFF_2_N]
#SYSTEM CLOCKS
set_property PACKAGE_PIN C25 [get_ports LVDS_OSC_P]
set_property IOSTANDARD LVDS_25 [get_ports LVDS_OSC_P]
set_property PACKAGE_PIN B25 [get_ports LVDS_OSC_N]
set_property IOSTANDARD LVDS_25 [get_ports LVDS_OSC_N]
#LEDs
set_property PACKAGE_PIN A20 [get_ports APP_LED1]
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set_property IOSTANDARD LVCMOS18 [get_ports APP_LED1]
set_property PACKAGE_PIN A17 [get_ports APP_LED2]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED2]
set_property PACKAGE_PIN A16 [get_ports APP_LED3]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED3]
set_property PACKAGE_PIN B20 [get_ports APP_LED4]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED4]
set_property PACKAGE_PIN C20 [get_ports APP_LED5]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED5]
set_property PACKAGE_PIN F17 [get_ports APP_LED6]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED6]
set_property PACKAGE_PIN G17 [get_ports APP_LED7]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED7]
set_property PACKAGE_PIN B17 [get_ports APP_LED8]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED8]
#IIC
set_property PACKAGE_PIN F21 [get_ports DUT_I2C_SCL]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_I2C_SCL]
set_property PACKAGE_PIN E21 [get_ports DUT_I2C_SDA]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_I2C_SDA]
#PMBUS
set_property PACKAGE_PIN C21 [get_ports DUT_PMB_ALERT]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_ALERT]
set_property PACKAGE_PIN D21 [get_ports DUT_PMB_CTRL]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_CTRL]
set_property PACKAGE_PIN H22 [get_ports DUT_PMB_CLK]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_CLK]
set_property PACKAGE_PIN H21 [get_ports DUT_PMB_DATA]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_DATA]
#UART-GPIO
set_property PACKAGE_PIN L17 [get_ports USB_GPIO_0]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_0]
set_property PACKAGE_PIN H19 [get_ports USB_GPIO_1]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_1]
set_property PACKAGE_PIN J19 [get_ports USB_GPIO_2]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_2]
set_property PACKAGE_PIN H17 [get_ports USB_GPIO_3]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_3]
#UART
set_property PACKAGE_PIN J17 [get_ports USB_TXD_0]
set_property IOSTANDARD LVCMOS18 [get_ports USB_TXD_0]
set_property PACKAGE_PIN G20 [get_ports USB_RXD_I]
set_property IOSTANDARD LVCMOS18 [get_ports USB_RXD_I]
set_property PACKAGE_PIN H20 [get_ports USB_RTS_0_B]
set_property IOSTANDARD LVCMOS18 [get_ports USB_RTS_0_B]
set_property PACKAGE_PIN J18 [get_ports USB_CTS_I_B]
set_property IOSTANDARD LVCMOS18 [get_ports USB_CTS_I_B]
#SDIO
set_property PACKAGE_PIN G18 [get_ports SA2_SDHOST_D0]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D0]
set_property PACKAGE_PIN C16 [get_ports SA2_SDHOST_D1]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D1]
set_property PACKAGE_PIN D16 [get_ports SA2_SDHOST_D2]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D2]
set_property PACKAGE_PIN D19 [get_ports SA2_SDHOST_D3]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D3]
set_property PACKAGE_PIN L18 [get_ports SA2_SDHOST_CMD]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_CMD]
set_property PACKAGE_PIN E19 [get_ports SA2_SDHOST_CLK]
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set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_CLK]
#QSPI
set_property PACKAGE_PIN E28 [get_ports GTX_MOD_SPI_SCK]
set_property IOSTANDARD LVCMOS18 [get_ports GTX_MOD_SPI_SCK]
set_property PACKAGE_PIN D27 [get_ports GTX_MOD_SPI_D]
set_property IOSTANDARD LVCMOS18 [get_ports GTX_MOD_SPI_D]
set_property PACKAGE_PIN C27 [get_ports GTX_MOD_SPI_Q]
set_property IOSTANDARD LVCMOS18 [get_ports GTX_MOD_SPI_Q]
set_property PACKAGE_PIN D28 [get_ports GTX_MOD_SPI_CS]
set_property IOSTANDARD LVCMOS18 [get_ports GTX_MOD_SPI_CS]
#MGTs
set_property PACKAGE_PIN R8 [get_ports 115_REFCLK0_P]
set_property PACKAGE_PIN R7 [get_ports 115_REFCLK0_N]
set_property PACKAGE_PIN U8 [get_ports 115_REFCLK1_P]
set_property PACKAGE_PIN U7 [get_ports 115_REFCLK1_N]
set_property PACKAGE_PIN T2 [get_ports 115_TX3_P]
set_property PACKAGE_PIN T1 [get_ports 115_TX3_N]
set_property PACKAGE_PIN V6 [get_ports 115_RX3_P]
set_property PACKAGE_PIN V5 [get_ports 115_RX3_N]
set_property PACKAGE_PIN U4 [get_ports 115_TX2_P]
set_property PACKAGE_PIN W4 [get_ports 115_RX2_P]
set_property PACKAGE_PIN U3 [get_ports 115_TX2_N]
set_property PACKAGE_PIN W3 [get_ports 115_RX2_N]
set_property PACKAGE_PIN V2 [get_ports 115_TX1_P]
set_property PACKAGE_PIN V1 [get_ports 115_TX1_N]
set_property PACKAGE_PIN Y6 [get_ports 115_RX1_P]
set_property PACKAGE_PIN Y5 [get_ports 115_RX1_N]
set_property PACKAGE_PIN Y2 [get_ports 115_TX0_P]
set_property PACKAGE_PIN Y1 [get_ports 115_TX0_N]
set_property PACKAGE_PIN AA4 [get_ports 115_RX0_P]
set_property PACKAGE_PIN AA3 [get_ports 115_RX0_N]
set_property PACKAGE_PIN L8 [get_ports 116_REFCLK0_P]
set_property PACKAGE_PIN L7 [get_ports 116_REFCLK0_N]
set_property PACKAGE_PIN N8 [get_ports 116_REFCLK1_P]
set_property PACKAGE_PIN N7 [get_ports 116_REFCLK1_N]
set_property PACKAGE_PIN L4 [get_ports 116_TX3_P]
set_property PACKAGE_PIN L3 [get_ports 116_TX3_N]
set_property PACKAGE_PIN M6 [get_ports 116_RX3_P]
set_property PACKAGE_PIN M5 [get_ports 116_RX3_N]
set_property PACKAGE_PIN M2 [get_ports 116_TX2_P]
set_property PACKAGE_PIN M1 [get_ports 116_TX2_N]
set_property PACKAGE_PIN P6 [get_ports 116_RX2_P]
set_property PACKAGE_PIN P5 [get_ports 116_RX2_N]
set_property PACKAGE_PIN N4 [get_ports 116_TX1_P]
set_property PACKAGE_PIN N3 [get_ports 116_TX1_N]
set_property PACKAGE_PIN R4 [get_ports 116_RX1_P]
set_property PACKAGE_PIN R3 [get_ports 116_RX1_N]
set_property PACKAGE_PIN P2 [get_ports 116_TX0_P]
set_property PACKAGE_PIN P1 [get_ports 116_TX0_N]
set_property PACKAGE_PIN T6 [get_ports 116_RX0_P]
set_property PACKAGE_PIN T5 [get_ports 116_RX0_N]
set_property PACKAGE_PIN G8 [get_ports 117_REFCLK0_P]
set_property PACKAGE_PIN G7 [get_ports 117_REFCLK0_N]
set_property PACKAGE_PIN J8 [get_ports 117_REFCLK1_P]
set_property PACKAGE_PIN J7 [get_ports 117_REFCLK1_N]
set_property PACKAGE_PIN F2 [get_ports 117_TX3_P]
set_property PACKAGE_PIN F1 [get_ports 117_TX3_N]
set_property PACKAGE_PIN F6 [get_ports 117_RX3_P]
set_property PACKAGE_PIN F5 [get_ports 117_RX3_N]
```

```
set_property PACKAGE_PIN H2 [get_ports 117_TX2_P]
set_property PACKAGE_PIN H1 [get_ports 117_TX2_N]
set_property PACKAGE_PIN G4 [get_ports 117_RX2_P]
set_property PACKAGE_PIN G3 [get_ports 117_RX2_N]
set_property PACKAGE_PIN J4 [get_ports 117_TX1_P]
set_property PACKAGE_PIN J3 [get_ports 117_TX1_N]
set_property PACKAGE_PIN H6 [get_ports 117_RX1_P]
set_property PACKAGE_PIN H5 [get_ports 117_RX1_N]
set_property PACKAGE_PIN K2 [get_ports 117_TX0_P]
set_property PACKAGE_PIN K1 [get_ports 117_TX0_N]
set_property PACKAGE_PIN K6 [get_ports 117_RX0_P]
set_property PACKAGE_PIN K5 [get_ports 117_RX0_N]
set_property PACKAGE_PIN C8 [get_ports 118_REFCLK0_P]
set_property PACKAGE_PIN C7 [get_ports 118_REFCLK0_N]
set_property PACKAGE_PIN E8 [get_ports 118_REFCLK1_P]
set_property PACKAGE_PIN E7 [get_ports 118_REFCLK1_N]
set_property PACKAGE_PIN A4 [get_ports 118_TX3_P]
set_property PACKAGE_PIN A3 [get_ports 118_TX3_N]
set_property PACKAGE_PIN A8 [get_ports 118_RX3_P]
set_property PACKAGE_PIN A7 [get_ports 118_RX3_N]
set_property PACKAGE_PIN B2 [get_ports 118_TX2_P]
set_property PACKAGE_PIN B1 [get_ports 118_TX2_N]
set_property PACKAGE_PIN B6 [get_ports 118_RX2_P]
set_property PACKAGE_PIN B5 [get_ports 118_RX2_N]
set_property PACKAGE_PIN C4 [get_ports 118_TX1_P]
set_property PACKAGE_PIN C3 [get_ports 118_TX1_N]
set_property PACKAGE_PIN D6 [get_ports 118_RX1_P]
set_property PACKAGE_PIN D5 [get_ports 118_RX1_N]
set_property PACKAGE_PIN D2 [get_ports 118_TX0_P]
set_property PACKAGE_PIN D1 [get_ports 118_TX0_N]
set_property PACKAGE_PIN E4 [get_ports 118_RX0_P]
set_property PACKAGE_PIN E3 [get_ports 118_RX0_N]
```

VITA 57.1 FMC Connector Pinouts

Figure C-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

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Figure C-1: **FMC HPC Connector Pinout**

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Appendix D

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the KC724 board and its documentation is available on these websites:

Kintex-7 FPGA KC724 Characterization Kit

Kintex-7 FPGA KC724 Characterization Kit documentation

Kintex-7 FPGA KC724 Characterization Kit Answer Record (AR 43390)

These documents provide supplemental material useful with this guide:

1. *7 Series FPGAs Overview* DS180
2. *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* UG480
3. *Vivado Design Suite User Guide, Using Contstraints* UG903
4. *KC724 IBERT Getting Started Guide (ISE Design Suite)* UG930
5. *KC724 IBERT Getting Started Guide (Vivado Design Suite)* UG931
6. *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* DS182
7. *7 Series FPGAs Configuration User Guide* UG470
8. *7 Series FPGAs SelectIO Resources User Guide* UG471
9. *7 Series FPGAs Clocking Resources User Guide* UG472
10. *7 Series FPGAs Configurable Logic Block User Guide* UG474
11. *7 Series FPGAs Packaging and Pinout User Guide* UG475
12. *7 Series FPGAs GTX Transceivers User Guide* UG476
13. *7 Series FPGAs Integrated Block for PCI Express User Guide* PG054
14. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* UG770

These external websites provide supplemental material useful with this guide:

15. Texas Instruments Digital Power

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Appendix E

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Declaration of Conformity

To view the declaration of conformity online, visit:

Kintex-7 FPGA KC724 Declaration of Conformity

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product and can cause radio interference. In a domestic environment, the user might be required to take adequate corrective measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive.*