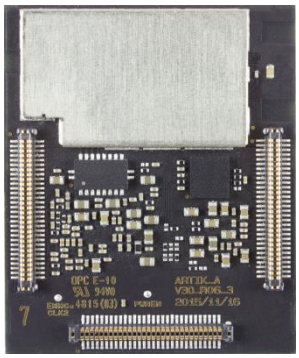
Samsung
ARTIK™

5

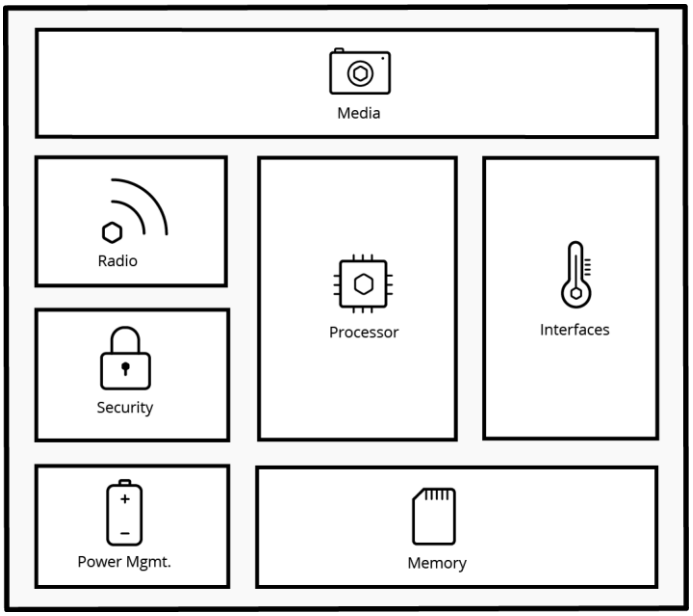
520 Data Sheet

TOP VIEW



BOTTOM VIEW

Samsung's ARTIK™ 520 Module is a highly-integrated System-in-Module that utilizes a dual core ARM® Cortex®-A7 processor packaged DRAM and Flash memories, a Secure Element and a wide range of wireless communication options such as 802.11a/b/g/n/ac, Bluetooth® 4.1, Bluetooth Low Energy (BLE), and 802.15.4/ZigBee® communications all into a 30x25mm footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module capabilities. With the combination of Wi-Fi, Bluetooth and ZigBee the ARTIK 520 Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability with the camera and display options. The hardware based Secure Element works with the ARM TrustZone® and Trustonic's Trusted Execution Environment (TEE) to provide "bank level" security end-to-end.



ARTIK 520 Module Block Diagram

Processor	
CPU	Dual core ARM® Cortex®-A7@1.0GHz
GPU	Mali™-400MP2 core
Media	
Camera I/F	1x 2-Lane MIPI CSI up to 3MP@30fps (Supports YUV and MJPEG format)
Display	2-Lane MIPI DSI up to qHD 960x540@24bpp
Audio	1-channel PCM and 1-channel 24-bit I²S audio interface
Memory	
DRAM	512MB LPDDR3
FLASH	4GB eMMC
Security	
Secure Element	Secure point to point authentication and data transfer
Trusted Execution Environment	Trustonic TEE (NDA required)
Radio	
WLAN	IEEE802.11a/b/g/n/ac
Bluetooth	BT, BLE
IEEE802.15.4	ZigBee
Power Management	
PMIC	Provides all power of the ARTIK 520 module using on board bucks and LDOs
Interfaces	
Analog and Digital I/O	GPIO, I²C, SPI, UART, SDIO, USB 2.0, JTAG, Analog Input

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VERSION HISTORY

Revision	Date	Description	Maturity
1.07	10/19/2016	ARTIK 520 Module Data Sheet	Release

ARTIK 520 Module Block Diagram

Figure 1 shows the functional block diagram of the ARTIK 520 Module. It consists of a dual-core ARM® Cortex®-A7 application processor with 512MB DRAM and 4GB eMMC Flash, PMIC, Secure Element, Wi-Fi/BT chipset, ZigBee chipset, RF connectors and socket-type connectors.

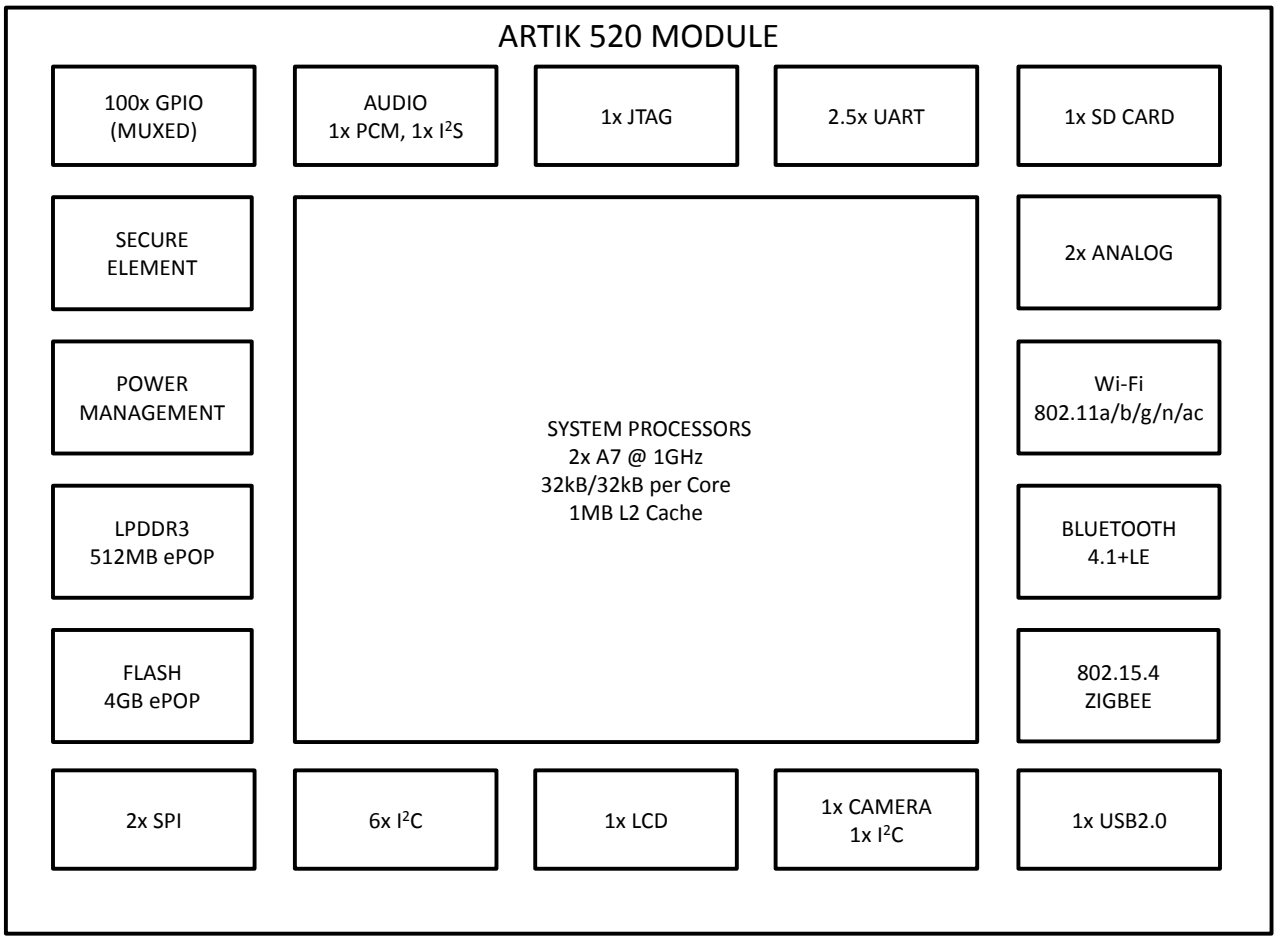

Figure 1. ARTIK 520 Module Functional Block Diagram

The top side is populated with the ARM® application processor, PMIC, Wi-Fi/BT combo chipset and RF connectors for Wi-Fi/BT and ZigBee antenna. The bottom side is populated with the ZigBee chipset, ZigBee front-end for RF and Secure Element, two main connectors for function connection to main set and one debug connector for debug interface connection.

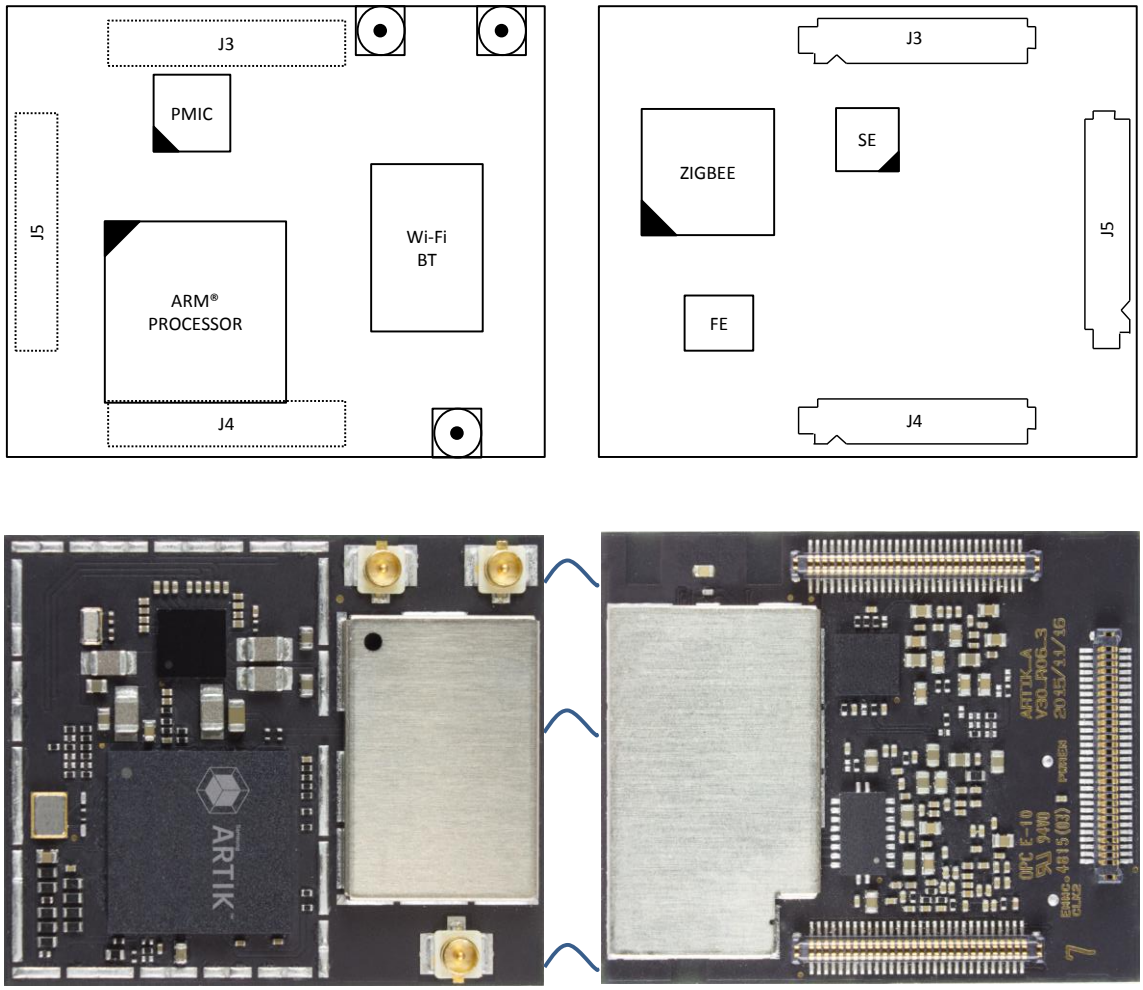

Figure 2. ARTIK 520 Module – Top View / Bottom View

ARTIK 520 Module ZigBee

The ARTIK 520 Module carries a fully-integrated ZigBee unit called the Ember® EM3587. It integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM® Cortex®-M3 microprocessor, flash and RAM memory and peripherals. The most important hardware features of the ZigBee module are:

- Complete system-on-chip using 32-bit ARM® Cortex®-M3 processor.
- Low power consumption:
  - RX current typical 27mA
  - TX current typical 31mA
  - Deep sleep current ≤ 1.25µA
- RF performance:
  - Normal mode link budget up to 110dB
  - RX sensitivity up to 102dBm
- Robust Wi-Fi and Bluetooth coexistence
- Single-voltage operation

For more information on EM3587 contact a sales representative from Silicon Laboratories, Inc.

ARTIK 520 Module ZigBee Front End

The ARTIK 520 Module carries a fully integrated RF Front-End Module (FEM) designed specifically for ZigBee Smart Energy IoT environments. The device provides integrated and fully matched input baluns, an integrated inter-stage matching and harmonic filter, and digital controls compatible with 1.6 to 3.6 V CMOS levels. The RF blocks of the SE2432L support a wide range supply voltage tailored toward battery operated environments. The most important hardware features of the ZigBee front-end are:

- Integrated Power Amplifier up to 24dBm
- Integrated Low-Noise Amplifier with programmable bypass
- Integrated antenna switching, with transmit and receive diversity function
- Low NF, 2dB typical
- Differential transmit/receive interface with integrated baluns
- Fast-switch on/off time ≤ 800ns
- Sleep-mode current ≤ 0.05µA

For more information on SE2432L contact a sales representative from Skyworks Solutions, Inc.

ARTIK 520 Module PMIC

The ARTIK 520 Module has a fully-integrated PMIC containing 5 Bucks and 25 LDOs. This unit provides all power requirements for the ARTIK 520 Module in one compact form factor. In addition, various stable power outputs are offered at the connectors, such that additional customer-defined use cases can be defined and efficiently implemented.

For more information on S2MPS14 contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 520 Module Wi-Fi/Bluetooth

The ARTIK 520 Module has a fully-integrated MIMO combo BCM4354 for IEEE 802.11 a/b/g/n/ac wireless LAN with Bluetooth 4.0+LE and FM. The most important hardware features of the Wireless/Bluetooth combo module are:

- WLAN 802.11ac compliant:
  - Single-stream spatial multiplexing up to 433Mbps
  - Support for 20, 40 and 80 MHz channels with optional SGI (256 QAM modulation)
- WLAN 802.11 a/b/g/n/ac compliant
- Bluetooth 4.0+LE
- 2G and 5G MIMO support
- FM Receiver, 65MHz-108MHz bands

For more information on BCM 4354 contact a sales representative from Broadcom Ltd.

ARTIK 520 Module Secure Element

The ARTIK 520 Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The most important hardware features of the Secure Element are:

- Dedicated secure CPU SC300
- Crypto Accelerator
  - Hardware based AES/DES/3DES
  - TORNADO-E
  - 5KB crypto RAM
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 4128bits/ECC 544 bits
- Data security
  - Abnormal-condition detectors for: reset, interrupt, voltage, temperature, laser exposure, shield removal
  - Random Wait Generator, Random Current Generator
  - Secure optimized layout
  - Dynamic bus encryption
- Embedded tamper-free memory
  - 1.5MB flash (program and data)
  - 32KB MASK ROM
  - 48KB Static RAM
  - 5KB Crypto RAM
  - Memory Protection Unit with 4GB addressable space
  - Secure flash write operation with fast page (0.5ms) and sector erase (4ms)
  - 500K erase/write cycles/s
- Serial interfaces:
  - I^2C/SPI/UART (ISO 7816)
- A guaranteed 25 years data retention at room temperature

For more information on S3FV5RP contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 520 Module Secure JTAG

Our secure JTAG core that is part of the ARTIK 520 Module provides debug capabilities for the developer. The secure JTAG core authenticates the legal user. In addition, it provides an access level that the legal user can operate under. The main features of the secure JTAG core are:

- Dedicated authentication process through password
- Dedicated Hash engine (SHA-1) with hash sequencer
- Two access levels “access-on” and “access-off”
- Industry standard JTAG capabilities

ARTIK 520 Module Processor System

The processor system architecture that resides on the ARTIK 520 Module is a system-on-a-chip (SoC) based on a 32-bit RISC processor. Designed using the 28nm low power process, the processor system architecture provides superior performance using a dual-core CORTEX®-A7 CPU. The ARTIK 520 Module contains 3D graphics hardware, image signal-processor hardware and a variety of high-speed interfaces such as eMMC5.0.

The ARTIK 520 Module contains the dual Cortex®-A7. The ARTIK 520 Module allows for heavy traffic operations such as
720p video encoding/decoding, 3D graphics display and high resolution image signal processing.

The application processor supports dynamic virtual-address mapping aiding software engineers to fully utilize the memory resources. The key features of the ARTIK 520 Module are:

- Dual-core ARM® Cortex®-A7, 32 KB I$/32 KB D$ and 1MB L2 Cache
- 128-bit multi-layer AXI bus architecture
- Internal ROM and RAM for secure booting and general-use purposes
- Memory subsystem:
  - 1-port 32-bit 400MHz LPDDR2/LPDDR3 interface
- Supports 3D and 2D graphics hardware
- LCD single qHD display supports MIPI
- Support for 2-lane MIPI DSI interface
- Support for 2-lane MIPI CSI interface
- Support for 1-channel PCM and 1-channel 24-bit I^2S audio interface
- Support for 6-channel I^2C general-purpose multi-master interface and 1-channel dedicated camera I^2C interface
- Support for 2-channel high-speed SPI interface
- Support for 2.5-channel high-speed UART (up to 3Mbps data rate for Bluetooth 2.1 EDR and IrDA 1.0 SIR)
- Support for USB 2.0, 1-channel supports LS/FS/HS (1.5Mbps/12Mbps/480Mbps) with on-chip PHY
- Support for 2-channel SD/MMC interface supports SDIO3.0, eMMC5.0 DDR with 8-bit interface
- Support for up to 100 configurable GPIO (multiplexed)
- Real time clock, PLLs, timer with PWM, and watchdog timer
- Support for 2-channel (multiplexed) general-purpose ADC

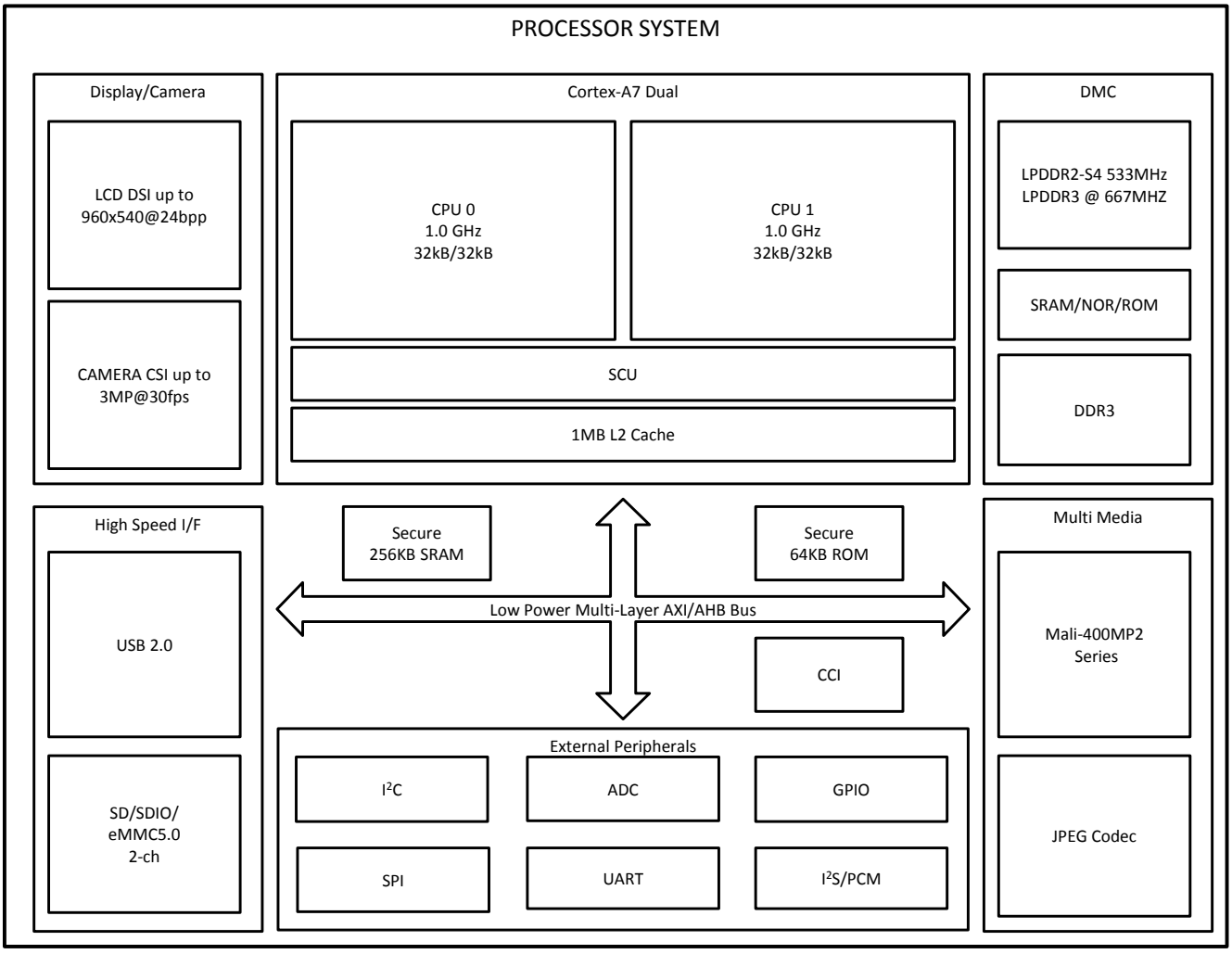

Figure 3. Processor System Block Schematic

MIPI DSI

The ARTIK 520 Module provides 1x 2-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are:

- Maximum resolution ranges up to qHD (960x540@24bpp)
- Supports 1 or 2 data lanes.
- Supported interfaces are:
  - Protocol-to-PHY Interface (PPI) in MIPI D-PHY specification V0.90
  - RGB Interface for video image input from display controller
  - An I80 interface for Command Mode Image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Pre-scaler to generate escape clock from byte clock

MIPI CSI

The ARTIK 520 Module provides 1x 2-lane MIPI interface that complies with the MIPI CSI standard specification V1.01r06. The key features of the MIPI CSI sub-system are:

- Supports 1 or 2 data lanes

- Supports up to 3MP@30fps
- Supported image formats are:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - MJPEG

SPI

The ARTIK 520 Module provides 2x Serial Peripheral Interfaces (SPI) that transfers serial data. SPI support includes
8-bit/16-bit/32-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by National Semiconductor, Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full-duplex
- 8-bit/16-bit/32-bit shift register for Tx and Rx
- 8-bit/16-bit/32-bit bus interface
- Complies with the SPI protocol described by National Semiconductor, Microwire and Motorola
- Support for 2 independent 32-bit wide transmit and receive FIFOs:
  - Depth 64 in SPI port 0 and depth 16 in SPI port 1
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Support Tx/Rx up to 50 MHz

ADC

The ADC interface controls one 28nm low power CMOS 1.8V 12-bit ADC. It converts the analog input signal into 12-bit binary code at a conversion rate of 50kSPS-1MSPS with a 1MHz-20MHz main clock. The ADCIF includes a 12-bit resolution that combines with an analog input multiplexer. The analog input multiplexer selects one from 2 input channels.

UART

The ARTIK 520 Module provides 2x full 4-pin UARTs plus 1x 2-pin UART with just RxD and TxD signals. The key features of the UART sub-system are:

- Both DMA and interrupt based mode of operation supported
- All independent channels support IrDA 1.0
- Each UART channel contains two FIFOs to receive and transmit data:
  - 256 bytes in ch0 and ch2
  - 64 bytes in ch1
  - 16 bytes in ch3
- Each UART channel contains:
  - Programmable baud-rates
  - One or two stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

I^2S

The ARTIK 520 Module provides one 3-line Inter-IC Sound (I^2S) channel. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as sub-coding and control.

It is possible to transmit data between two I^2S buses. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used. The key features of the I^2S sub-system are:

- Supports 1-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Supports serial data transfer of 8/16/24-bit per channel
- Supports I^2S, MSB-justified, and LSB-justified data formats
- Supports both master and slave modes

PCM

The ARTIK 520 Module provides 1x PCM channel. The PCM audio interface provides a bi-directional serial interface
to an external codec. The key features of the PCM sub-system are:

- A 16-bit PCM with 1 port audio interface
- Supports only Master mode
- All PCM serial timings and strobes are extracted from one master clock
- Supports 1x input (16-bit x 32depth) and 1x output (16-bit x 32 depth) FIFO to buffer data
- DMA interface for Tx or Rx or both

GPIO

The ARTIK 520 Module provides a GPIO system to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- Control for up to 91 external interrupts
  - Falling edge triggered
  - Rising edge triggered
  - Both edge triggered
- Control for up to 25 wake-up interrupts
  - Falling edge triggered
  - Rising edge triggered
  - Both edge triggered
- Control for up to 100 General Purpose I/Os
- Controls a variety of pin states in sleep mode

I^2C

The ARTIK 520 Module provides 6x generic 400kb/s I^2C channels + 1x dedicated 400kb/s camera I^2C channel. The key features of the I^2C sub-system are:

- Supporting master and slave mode
- 7-bit addressing mode only
- Supports serial, 8-bit oriented and bi-directional data transfer
- Supports up to 100 kb/s in the standard mode
- Supports up to 400 kb/s in the fast mode
- Supports master transmit, master receive, slave transmit, and slave receive operation
- Supports both interrupt and polling events

USB

The ARTIK 520 Module provides one USB2.0 interface. The key features of the USB2.0 sub-system are:

- In compliance with the USB 2.0 specification revision 1.0a
- In compliance with the UTMI+ Level3 revision 1.0
- Supports high-speed and full-speed transfers
- Supports up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction

- Supports packet-based dynamic FIFO memory allocation up to 7936 depth

SDIO/xMMC

The ARTIK 520 Module provides one SDIO/xMMC interface. The Mobile Storage Host is an interface between the system and SD/MMC card. This host supports 8-bit DDR transfer with a 200 MHz clock rate. The key features of mobile storage host sub-system are:

- Support for Embedded Multimedia Cards (eMMC – version 5.0)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- Support for Multimedia Cards (MMC – version 4.4)

Mali™-400 Series

The ARTIK 520 Module provides 1x instance of the Mali™-400 GPU series from ARM®. The Mali™-400 series adds graphics capabilities to the ARTIK 520 Module. The key features of the Mali™-400 sub-system are:

- Resolution of 4kx4k for the frame buffer as well as the texture buffer
- Tile-based pixel processing
- Scalable multi-core pixel processors (128 threads)

DMC

The ARTIK 520 Module provides a Dynamic Memory Controller (DMC) that is compatible with the JEDEC standard supporting LPDDR3/DDR3 and SDRAM devices. The following memory interfaces are supported:

- LPDDR2-S4 up to 533MHz
- LPDDR3 up to 667 MHz
- DDR3

Dual Cortex®-A7

The ARTIK 520 Module provides 2xCPU cores which consist of ARM® Cortex®-A7 core processors. For easier and faster CPU core switching, the ARTIK 520 Module supports a cache coherency interconnect (CCI) bus with L2 cache snooping capability. The ARM® Cortex®-A7 dual-core has the following common features:

- Common ARM®v7-A Cortex® architecture
- A core speed up to 1GHZ
- Security Extensions for implementation of enhanced security
- Virtualization Extensions for the development of virtualized systems that enable switching guest operation systems
- Program Trace Macrocell that is ARM CoreSight compatible
- Multi-core ARM TrustZone® technology

ARTIK 520 Module Connectors

The ARTIK 520 Module utilizes three 60-position connectors for all power, analog and digital I/O. Connectors J3, J4 and J5 are Panasonic ATX460124 with 60 pins and 0.4mm pitch. *Figure 4* shows the power/signal name assigned to each pin of each connector. *Table 1*, *Table 2* and *Table 3* describe the pinout in detail.

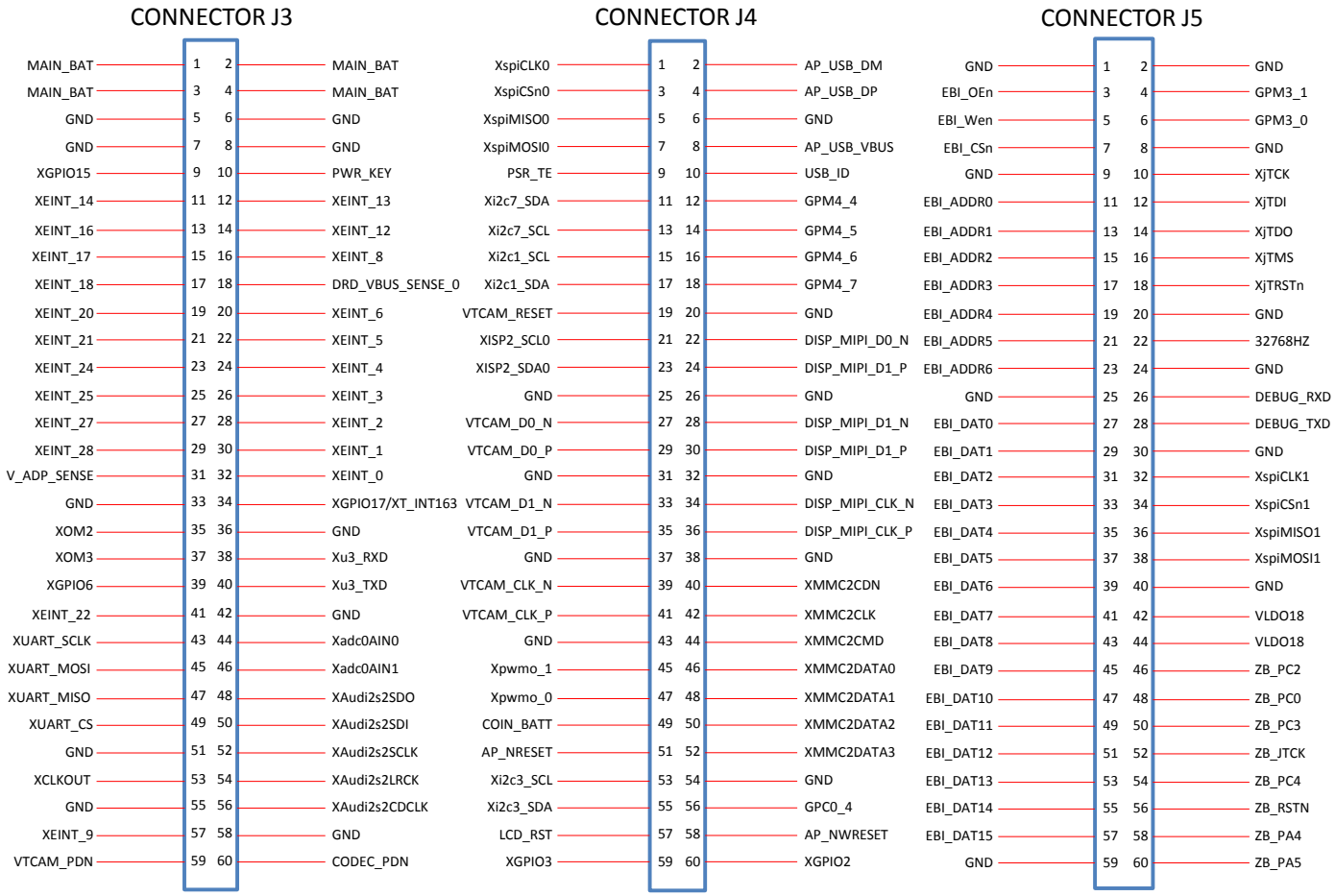

Figure 4. ARTIK 520 Module Connectors

CONNECTOR J3

Table 1. Connector J3

Connector J3									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD*	Group	Function
J3	1	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	3	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	5	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	7	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	9	XGPIO15	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip GPIO1
J3	11	XEINT_14	I	A	1V8	2	PUE	ARDUINO	General purpose interrupt or IO
J3	13	XEINT_16	I	A	1V8	2	PUD D	ETHERNET CONTROLLER	External chip IRQ
J3	15	XEINT_17	I	A	1V8	2	PUD D	POWER/RESET	Charge status interrupt
J3	17	XEINT_18	I	A	1V8	2	PUD D	UART	SPI-TO-UART IC for SPI bus emulation RESET
J3	19	XEINT_20	I	A	1V8	2	PUD D	UART	SPI-TO-UART IC for SPI bus emulation IRQ
J3	21	XEINT_21	O	A	1V8	2	PUD D	LCD	Backlight enable
J3	23	XEINT_24	I	A	1V8	2	PDE	POWER/RESET	Turn device on
J3	25	XEINT_25	I	A	1V8	2	PDE	POWER/RESET	Fuel gauge interrupt
J3	27	XEINT_27	I	A	1V8	2	PDE	AUDIO	Ear microphone detect
J3	29	XEINT_28	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip CS
J3	31	V_ADP_SENSE	I	A/SE	1V8	2	PDE	POWER/RESET	AC Power detect
J3	33	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	35	XOM2	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	37	XOM3	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	39	XGPIO6	I	A	1V8	2	PDE	ZWAVE	SD3503 ZWAVE reset
J3	41	XEINT_22	I	A	1V8	2	PUD D	CAMERA	27MHz osc enable
J3	43	XUART_SCLK	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation SCLK
J3	45	XUART_MOSI	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MOSI
J3	47	XUART_MISO	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MISO
J3	49	XUART_CS	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation CS
J3	51	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	53	XCLKOUT	O	PROCESSOR	1V8	NA	NA	AUDIO	Clock
J3	55	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	57	XEINT_9	I	A	1V8	2	PDE	ETHERNET CONTROLLER	General purpose interrupt or IO
J3	59	VTCAM_PDN	I	A	1V8	2	PDE	CAMERA	Power down
J3	2	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	4	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	6	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	8	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	10	PWR_KEY	I	PMIC	NA	NA	NA	POWER/RESET	PMIC power on key

Connector J3									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD*	Group	Function
J3	12	XEINT_13	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	14	XEINT_12	I	A	1V8	2	PDE	SIGFOX	Low power wireless transmitter reset
J3	16	XEINT_8	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	18	DRD_VBUS_SENSE_0	I	A	1V8	2	PDE	USB	Device detect
J3	20	XEINT_6	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	22	XEINT_5	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	24	XEINT_4	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	26	XEINT_3	I	A	1V8	2	PUE	ARDUINO	General purpose interrupt or IO
J3	28	XEINT_2	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	30	XEINT_1	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	32	XEINT_0	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	34	XGPIO17/XT_INT163	I	A	1V8	2	PDE	POWER/RESET	External IC interrupt
J3	36	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	38	Xu3_RXD	I	A	1V8	2	PUDD	ARDUINO	RxD
J3	40	Xu3_TXD	I	A	1V8	2	PUDD	ARDUINO	TxD
J3	42	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	44	Xadc0AIN0	I	ADC	1V8	NA	NA	ARDUINO	Input 0
J3	46	Xadc0AIN1	I	ADC	1V8	NA	NA	ARDUINO	Input 1
J3	48	XAudi2s2SDO	I	A	1V8	2	PDE	AUDIO	SDO
J3	50	XAudi2s2SDI	I	A	1V8	2	PDE	AUDIO	SDI
J3	52	XAudi2s2SCLK	I	A	1V8	2	PDE	AUDIO	SCLK
J3	54	XAudi2s2LRCK	I	A	1V8	2	PDE	AUDIO	LRCLK
J3	56	XAudi2s2CDCLK	I	A	1V8	2	PDE	AUDIO	CDCLK
J3	58	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	60	CODEC_PDN	I	A	1V8	2	PDE	AUDIO	AK4953EQ audio codec IC power down

* The PUD variables have the following meaning: PUDD = Power Up Down Disabled, PDE = Power Down Enabled, PUE = Power Up Enabled, R = Reserved.

CONNECTOR J4

Table 2. Connector J4

Connector J4									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	1	XspiCLK0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI CLK
J4	3	XspiCSn0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI CSn
J4	5	XspiMISO0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI MISO
J4	7	XspiMOSI0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI MOSI
J4	9	PSR_TE	I	A	1V8	2	PDE	LCD	CLK
J4	11	Xi2c7_SDA	I	A	1V8	2	PDE	ARDUINO	General purpose I2C SDA
J4	13	Xi2c7_SCL	I	A	1V8	2	PDE	ARDUINO	General purpose I2C SCL
J4	15	Xi2c1_SCL	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SCL
J4	17	Xi2c1_SDA	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SDA
J4	19	VTCAM_RESET	O	A	1V8	2	PDE	CAMERA	RESET Camera
J4	21	XISP2_SCL0	I	A	1V8	2	PDE	CAMERA	I2C SCL
J4	23	XISP2_SDA0	I	A	1V8	2	PDE	CAMERA	I2C SDA
J4	25	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	27	VTCAM_D0_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_N
J4	29	VTCAM_D0_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_P
J4	31	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	33	VTCAM_D1_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_N
J4	35	VTCAM_D1_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_P
J4	37	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	39	VTCAM_CLK_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_N
J4	41	VTCAM_CLK_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_P
J4	43	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	45	Xpwmo_1	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO or PWM
J4	47	Xpwmo_0	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO or PWM
J4	49	COIN_BAT	NA	PMIC	3V0	NA	NA	POWER/RESET	Backup battery
J4	51	AP_NRESET	I	PROCESSOR/PMIC	1V8	NA	NA	POWER/RESET/ ARDUINO/JTAG	ARTIK 520 Module reset
J4	53	Xi2c3_SCL	I	A	1V8	2	PUDD	TEST POINTS	I2C SCL
J4	55	Xi2c3_SDA	I	A	1V8	2	PUDD	TEST POINTS	I2C SDA
J4	57	LCD_RST	O	A	1V8	2	PDE	LCD	Reset
J4	59	XGPIO3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External Chip GPIO0
J4	2	AP_USB_DM	I/O	USB2.0	3V0	NA	NA	USB	USB DM
J4	4	AP_USB_DP	I/O	USB2.0	3V0	NA	NA	USB	USB DP
J4	6	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	8	AP_USB_VBUS	I/O	USB2.0	3V0	NA	NA	USB	USB VBUS
J4	10	USB_ID	I	USB2.0	3V0	NA	NA	USB	ID
J4	12	GPM4_4	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	14	GPM4_5	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	16	GPM4_6	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	18	GPM4_7	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	20	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	22	DISP_MIPI_D0_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_N

Connector J4									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	24	DISP_MIPI_D0_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_P
J4	26	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	28	DISP_MIPI_D1_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_N
J4	30	DISP_MIPI_D1_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_P
J4	32	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	34	DISP_MIPI_CLK_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_N
J4	36	DISP_MIPI_CLK_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_P
J4	38	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	40	XMMC2CDN	I	B	1V8	4	PUE	SD CARD	XMMC2 CDN
J4	42	XMMC2CLK	O	B	1V8	12	PUDD	SD CARD	XMMC2 CLK
J4	44	XMMC2CMD	O	B	1V8	12	PUDD	SD CARD	XMMC2 CMD
J4	46	XMMC2DATA0	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA0
J4	48	XMMC2DATA1	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA1
J4	50	XMMC2DATA2	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA2
J4	52	XMMC2DATA3	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA3
J4	54	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	56	GPC0_4	I	A	1V8	2	PDE	LCD	Identification (ID)
J4	58	AP_NWRESET	I	PROCESSOR/PMIC	1V8	NA	NA	PMIC	Warm reset from PMIC (development purposes)
J4	60	XGPIO2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip reset

CONNECTOR J5

Table 3. Connector J5

Connector J5									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J5	1	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	3	EBI_OEn	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip RDN
J5	5	EBI_Wen	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip WRN
J5	7	EBI_CSn	I	A	1V8	2	PDE	ETHERNET CONTROLLER	CS 1 default connect
J5	9	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	11	EBI_ADDR0	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR0
J5	13	EBI_ADDR1	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR1
J5	15	EBI_ADDR2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR2
J5	17	EBI_ADDR3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR3
J5	19	EBI_ADDR4	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR4
J5	21	EBI_ADDR5	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR5
J5	23	EBI_ADDR6	I	A	1V8	2	PDE	NA	Not used
J5	25	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	27	EBI_DAT0	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 0
J5	29	EBI_DAT1	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 1
J5	31	EBI_DAT2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 2
J5	33	EBI_DAT3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 3
J5	35	EBI_DAT4	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 4
J5	37	EBI_DAT5	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 5
J5	39	EBI_DAT6	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 6
J5	41	EBI_DAT7	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 7
J5	43	EBI_DAT8	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 8
J5	45	EBI_DAT9	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 9
J5	47	EBI_DAT10	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 10
J5	49	EBI_DAT11	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 11
J5	51	EBI_DAT12	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 12
J5	53	EBI_DAT13	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 13
J5	55	EBI_DAT14	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 14
J5	57	EBI_DAT15	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 15
J5	59	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	2	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	4	GPM3_1	I	A	1V8	2	PDE	TEST POINTS	Not used
J5	6	GPM3_0	I	A	1V8	2	PDE	TEST POINTS	Not used
J5	8	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	10	XjTCK	I	JTAG	1V8	NA	NA	JTAG	JTAG CLK
J5	12	XjTDI	I	JTAG	1V8	NA	NA	JTAG	JTAG TDI
J5	14	XjTDO	O	JTAG	1V8	NA	NA	JTAG	JTAG TDO
J5	16	XjTMS	I	JTAG	1V8	NA	NA	JTAG	JTAG TMS
J5	18	XjTRSTn	I	JTAG	1V8	NA	NA	JTAG	JTAG RSTn
J5	20	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	22	32768HZ	O	PROCESSOR/PMIC/BT	1V8	NA	NA	TEST POINTS	32 KHz clock
J5	24	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	26	DEBUG_RXD	I	A	1V8	2	PUDD	DEBUG	AP debug UART RxD
J5	28	DEBUG_TXD	I	A	1V8	2	PUDD	DEBUG	AP debug UART TxD
J5	30	GND	NA	NA	0V0	NA	NA	NA	Ground

Connector J5									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J5	32	XspiCLK1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI CLK
J5	34	XspiCSn1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI CSn
J5	36	XspiMISO1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI MISO
J5	38	XspiMOSI1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI MOSI
J5	40	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	42	VLDO18	NA	NA	2V8	NA	NA	JTAG	2.8V/300mA
J5	44	VLDO18	NA	NA	2V8	NA	NA	JTAG	2.8V/300mA
J5	46	ZB_PC2	O	ZIGBEE	1V8	NA	NA	JTAG	JTAG data out
J5	48	ZB_PC0	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG reset
J5	50	ZB_PC3	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG data in
J5	52	ZB_JTCK	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG clock
J5	54	ZB_PC4	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG mode select
J5	56	ZB_RSTn	O	ZIGBEE/LS	1V8	2	PDE	JTAG	JTAG reset
J5	58	ZB_PA4	I/O	ZIGBEE	1V8	NA	NA	JTAG	JTAG GPIO
J5	60	ZB_PA5	I/O	ZIGBEE/LS	1V8	NA	NA	JTAG	JTAG GPIO

ARTIK 520 Module Functional Interfaces

This section shows the functional interfaces that are available at the connectors. Since some of the functionality is spread over multiple connectors, these tables will help provide better insight into what functionality is located where. The functions provided are related to the development environment used. Depending on your project you can always choose to reprogram some of the GPIOs that are currently assigned to the functional interfaces as described below.

USB

Table 4. USB

USB									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	18	DRD_VBUS_SENSE_0	I	A	1V8	2	PDE	USB	Device detect
J4	2	AP_USB_DM	I/O	USB2.0	3V0	NA	NA	USB	USB DM
J4	4	AP_USB_DP	I/O	USB2.0	3V0	NA	NA	USB	USB DP
J4	8	AP_USB_VBUS	I/O	USB2.0	3V0	NA	NA	USB	USB VBUS
J4	10	USB_ID	I	USB2.0	3V0	NA	NA	USB	ID

Audio Codec

Table 5. Audio Codec

Audio Codec									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	27	XEINT_27	I	A	1V8	2	PDE	AUDIO	Ear microphone detect
J3	53	XCLKOUT	O	PROCESSOR	1V8	NA	NA	AUDIO	Clock
J3	48	XAudi2s2SDO	I	A	1V8	2	PDE	AUDIO	SDO
J3	50	XAudi2s2SDI	I	A	1V8	2	PDE	AUDIO	SDI
J3	52	XAudi2s2SCLK	I	A	1V8	2	PDE	AUDIO	SCLK
J3	54	XAudi2s2LRCK	I	A	1V8	2	PDE	AUDIO	LRCLK
J3	56	XAudi2s2CDCLK	I	A	1V8	2	PDE	AUDIO	CDCLK
J3	60	CODEC_PDN	I	A	1V8	2	PDE	AUDIO	AK4953EQ audio codec IC power down
J4	15	Xi2c1_SCL	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SCL
J4	17	Xi2c1_SDA	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SDA

UARTS

Table 6. UARTS

UARTS									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	17	XEINT_18	I	A	1V8	2	PUDD	UARTS	SPI-TO-UART IC for SPI bus emulation RESET
J3	19	XEINT_20	I	A	1V8	2	PUDD	UARTS	SPI-TO-UART IC for SPI bus emulation IRQ
J3	43	XUART_SCLK	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation SCLK
J3	45	XUART_MOSI	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MOSI
J3	47	XUART_MISO	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MISO
J3	49	XUART_CS	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation CS

CAMERA

Table 7. Camera

Camera									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	41	XEINT_22	I	A	1V8	2	PUDD	CAMERA	27MHz osc enable
J3	59	VTCAM_PDN	I	A	1V8	2	PDE	CAMERA	Power down
J4	19	VTCAM_RESET	O	A	1V8	2	PDE	CAMERA	RESET Camera
J4	21	XISP2_SCL0	I	A	1V8	2	PDE	CAMERA	I2C SCL
J4	23	XISP2_SDA0	I	A	1V8	2	PDE	CAMERA	I2C SDA
J4	27	VTCAM_D0_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_N
J4	29	VTCAM_D0_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_P
J4	33	VTCAM_D1_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_N
J4	35	VTCAM_D1_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_P
J4	39	VTCAM_CLK_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_N
J4	41	VTCAM_CLK_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_P

SD CARD

Table 8. SD Card

SD Card									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	40	XMMC2CDN	I	B	1V8	4	PUE	SD CARD	XMMC2 CDN
J4	42	XMMC2CLK	O	B	1V8	12	PUDD	SD CARD	XMMC2 CLK
J4	44	XMMC2CMD	O	B	1V8	12	PUDD	SD CARD	XMMC2 CMD
J4	46	XMMC2DATA0	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA0
J4	48	XMMC2DATA1	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA1
J4	50	XMMC2DATA2	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA2
J4	52	XMMC2DATA3	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA3

POWER/RESET

Table 9. Power/Reset

Power/Reset									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	15	XEINT_17	I	A	1V8	2	PUDD	POWER/RESET	Charge status interrupt
J3	23	XEINT_24	I	A	1V8	2	PDE	POWER/RESET	Turn device on
J3	25	XEINT_25	I	A	1V8	2	PDE	POWER/RESET	Fuel gauge interrupt
J3	31	V_ADP_SENSE	I	A/SE	1V8	2	PDE	POWER/RESET	AC Power detect
J3	35	XOM2	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	37	XOM3	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	10	PWR_KEY	I	PMIC	NA	NA	NA	POWER/RESET	PMIC power on key
J3	34	XGPIO17/XT_INT163	I	A	1V8	2	PDE	POWER/RESET	External IC interrupt
J4	49	COIN_BAT	NA	PMIC	3V0	NA	NA	POWER/RESET	Backup battery
J4	51	AP_NRESET	I	PROCESSOR/ PMIC	1V8	NA	NA	POWER/RESET/ ARDUINO/JTAG	ARTIK 520 Module reset

LCD

Table 10. LCD

LCD									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	21	XEINT_21	O	A	1V8	2	PUDD	LCD	Backlight enable
J4	9	PSR_TE	I	A	1V8	2	PDE	LCD	CLK
J4	57	LCD_RST	O	A	1V8	2	PDE	LCD	Reset
J4	22	DISP_MIPI_D0_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_N
J4	24	DISP_MIPI_D0_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_P
J4	28	DISP_MIPI_D1_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_N
J4	30	DISP_MIPI_D1_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_P
J4	34	DISP_MIPI_CLK_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_N
J4	36	DISP_MIPI_CLK_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_P
J4	56	GPC0_4	I	A	1V8	2	PDE	LCD	Identification (ID)

Ethernet Controller

Table 11. Ethernet Controller

Ethernet Controller									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	9	XGPIO15	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip GPIO1
J3	13	XEINT_16	I	A	1V8	2	PUD D	ETHERNET CONTROLLER	External chip IRQ
J3	29	XEINT_28	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip CS
J3	57	XEINT_9	I	A	1V8	2	PDE	ETHERNET CONTROLLER	General purpose interrupt or IO
J4	1	XspiCLK0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI CLK
J4	3	XspiCSn0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI CSn
J4	5	XspiMISO0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI MISO
J4	7	XspiMOSI0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI MOSI
J4	59	XGPIO3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External Chip GPIO0
J4	60	XGPIO2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip reset
J5	3	EBI_OEn	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip RDN
J5	5	EBI_Wen	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip WRN
J5	7	EBI_CSn	I	A	1V8	2	PDE	ETHERNET CONTROLLER	CS 1 default connect
J5	11	EBI_ADDR0	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR0
J5	13	EBI_ADDR1	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR1
J5	15	EBI_ADDR2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR2
J5	17	EBI_ADDR3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR3
J5	19	EBI_ADDR4	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR4
J5	21	EBI_ADDR5	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR5
J5	27	EBI_DAT0	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 0
J5	29	EBI_DAT1	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 1
J5	31	EBI_DAT2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 2
J5	33	EBI_DAT3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 3
J5	35	EBI_DAT4	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 4
J5	37	EBI_DAT5	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 5
J5	39	EBI_DAT6	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 6
J5	41	EBI_DAT7	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 7
J5	43	EBI_DAT8	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 8
J5	45	EBI_DAT9	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 9
J5	47	EBI_DAT10	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 10
J5	49	EBI_DAT11	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 11
J5	51	EBI_DAT12	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 12
J5	53	EBI_DAT13	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 13
J5	55	EBI_DAT14	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 14
J5	57	EBI_DAT15	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 15

ARDUINO

Table 12. Arduino

Arduino									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS	PUD	Group	Function
J3	11	XEINT_14	I	A	1V8	2	PUE	ARDUINO	General purpose interrupt or IO
J3	12	XEINT_13	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	16	XEINT_8	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	20	XEINT_6	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	22	XEINT_5	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	24	XEINT_4	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	26	XEINT_3	I	A	1V8	2	PUE	ARDUINO	General purpose interrupt or IO
J3	28	XEINT_2	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	30	XEINT_1	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	32	XEINT_0	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	38	Xu3_RXD	I	A	1V8	2	PUDD	ARDUINO	RxD
J3	40	Xu3_TXD	I	A	1V8	2	PUDD	ARDUINO	TxD
J3	44	Xadc0AIN0	I	ADC	1V8	NA	NA	ARDUINO	Input 0
J3	46	Xadc0AIN1	I	ADC	1V8	NA	NA	ARDUINO	Input 1
J4	11	Xi2c7_SDA	I	A	1V8	2	PDE	ARDUINO	General purpose I2C SDA
J4	13	Xi2c7_SCL	I	A	1V8	2	PDE	ARDUINO	General purpose I2C SCL
J4	45	Xpwmo_1	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO or PWM
J4	47	Xpwmo_0	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO or PWM

TEST POINTS

Table 13. Test Points

Test Points									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	53	Xi2c3_SCL	I	A	1V8	2	PUDD	TEST POINTS	I2C SCL
J4	55	Xi2c3_SDA	I	A	1V8	2	PUDD	TEST POINTS	I2C SDA
J5	4	GPM3_1	I	A	1V8	2	PDE	TEST POINTS	Not used
J5	6	GPM3_0	I	A	1V8	2	PDE	TEST POINTS	Not used
J5	22	32768HZ	O	PROCESSOR/PMIC/BT	1V8	NA	NA	TEST POINTS	32 KHz clock
J5	32	XspiCLK1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI CLK
J5	34	XspiCSn1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI CSn
J5	36	XspiMISO1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI MISO
J5	38	XspiMOSI1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI MOSI

SigFox

Table 14. SigFox

SigFox									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	14	XEINT_12	I	A	1V8	2	PDE	SIGFOX	Low power wireless transmitter reset
J4	12	GPM4_4	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	14	GPM4_5	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	16	GPM4_6	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	18	GPM4_7	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation

Debug

Table 15. Debug

Debug									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J5	10	XjTCK	I	JTAG	1V8	NA	NA	DEBUG	JTAG CLK
J5	12	XjTDI	I	JTAG	1V8	NA	NA	DEBUG	JTAG TDI
J5	14	XjTDO	O	JTAG	1V8	NA	NA	DEBUG	JTAG TDO
J5	16	XjTMS	I	JTAG	1V8	NA	NA	DEBUG	JTAG TMS
J5	18	XjTRSTn	I	JTAG	1V8	NA	NA	DEBUG	JTAG RSTn
J5	26	DEBUG_RXD	I	A	1V8	2	PUDD	DEBUG	AP debug UART RxD
J5	28	DEBUG_TXD	I	A	1V8	2	PUDD	DEBUG	AP debug UART TxD
J5	42	VLDO18	NA	NA	2V8	NA	NA	DEBUG	2.8V/300mA
J5	44	VLDO18	NA	NA	2V8	NA	NA	DEBUG	2.8V/300mA
J5	46	ZB_PC2	O	ZIGBEE	1V8	NA	NA	DEBUG	JTAG data out
J5	48	ZB_PC0	I	ZIGBEE	1V8	NA	NA	DEBUG	JTAG reset
J5	50	ZB_PC3	I	ZIGBEE	1V8	NA	NA	DEBUG	JTAG data in
J5	52	ZB_JTCK	I	ZIGBEE	1V8	NA	NA	DEBUG	JTAG clock
J5	54	ZB_PC4	I	ZIGBEE	1V8	NA	NA	DEBUG	JTAG mode select
J5	56	ZB_RSTn	O	ZIGBEE/LS	1V8	2	PDE	DEBUG	JTAG reset
J5	58	ZB_PA4	I/O	ZIGBEE	1V8	NA	NA	DEBUG	JTAG GPIO
J5	60	ZB_PA5	I/O	ZIGBEE/LS	1V8	NA	NA	DEBUG	JTAG GPIO

ARTIK 520 Module GPIO Alternate Functions

The Type A and Type B GPIOs as indicated in the connector tables have alternate functions that can be programmed using the GPIO API provided in the SW development environment. The tables below provide the alternate functions of all Type A and Type B GPIOs that are available on the edge connectors that are not connected to other components on the ARTIK 520 Module.

Table 16. Type A GPIO Alternate Functions Connector J3

Connector J3 Type A GPIO												
IO Group	Conn #	Pin#	Name	Default I/O	F1	F2	F3	F4	F5	F6	F7	F8
(gpe1-7)	J3	9	XGPIO15	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
(gpx1-6)	J3	11	XEINT_14	I	I	O	WAKEUP_INT1[6]	KP_COL[6]	Reserved	ALV_DBG[10]	Reserved	EXT_INT41[6]
(gpx2-0)	J3	13	XEINT_16	I	I	O	WAKEUP_INT2[0]	KP_ROW[0]	Reserved	ALV_DBG[12]	Reserved	EXT_INT42[0]
(gpx2-1)	J3	15	XEINT_17	I	I	O	WAKEUP_INT2[1]	KP_ROW[1]	Reserved	ALV_DBG[13]	Reserved	EXT_INT42[1]
(gpx2-2)	J3	17	XEINT_18	I	I	O	WAKEUP_INT2[2]	KP_ROW[2]	Reserved	ALV_DBG[14]	Reserved	EXT_INT42[2]
(gpx2-4)	J3	19	XEINT_20	I	I	O	WAKEUP_INT2[4]	KP_ROW[4]	Reserved	ALV_DBG[16]	Reserved	EXT_INT42[4]
(gpx2-5)	J3	21	XEINT_21	O	I	O	WAKEUP_INT2[5]	KP_ROW[5]	Reserved	ALV_DBG[17]	Reserved	EXT_INT42[5]
(gpx3-0)	J3	23	XEINT_24	I	I	O	WAKEUP_INT3[0]	KP_ROW[8]	Reserved	ALV_DBG[20]	Reserved	EXT_INT43[0]
(gpx3-1)	J3	25	XEINT_25	I	I	O	WAKEUP_INT3[1]	KP_ROW[9]	Reserved	ALV_DBG[21]	Reserved	EXT_INT43[1]
(gpx3-3)	J3	27	XEINT_27	I	I	O	WAKEUP_INT3[3]	KP_ROW[11]	Reserved	ALV_DBG[23]	Reserved	EXT_INT43[3]
(gpx3-4)	J3	29	XEINT_28	I	I	O	WAKEUP_INT3[4]	KP_ROW[12]	Reserved	ALV_DBG[24]	Reserved	EXT_INT43[4]
(gpe0-6)	J3	39	XGPIO6	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
(gpx2-6)	J3	41	XEINT_22	I	I	O	WAKEUP_INT2[6]	KP_ROW[6]	Reserved	ALV_DBG[18]	Reserved	EXT_INT42[6]
(gpm3-4)	J3	43	XUART_SCLK	I	I	O	CAM_GPIO[6]	nRTS_UART_ISP	Reserved	Reserved	Reserved	EXT_INT11[4]
(gpm3-5)	J3	45	XUART_MOSI	I	I	O	CAM_GPIO[7]	TXD_UART_ISP	Reserved	Reserved	Reserved	EXT_INT11[5]
(gpm3-6)	J3	47	XUART_MISO	I	I	O	CAM_GPIO[8]	nCTS_UART_ISP	Reserved	Reserved	Reserved	EXT_INT11[6]
(gpm3-7)	J3	49	XUART_CS	I	I	O	CAM_GPIO[9]	RXD_UART_ISP	Reserved	Reserved	Reserved	EXT_INT11[7]
(gpx1-1)	J3	57	XEINT_9	I	I	O	WAKEUP_INT1[1]	KP_COL[1]	Reserved	ALV_DBG[5]	Reserved	EXT_INT41[1]
(gpm0-2)	J3	59	VTCAM_PDN	I	I	O	CAM_BAY_RGB[1]	CAM_B_DATA[1]	Reserved	TraceData[1]	Reserved	EXT_INT8[2]
(gpx1-5)	J3	12	XEINT_13	I	I	O	WAKEUP_INT1[5]	KP_COL[5]	Reserved	ALV_DBG[9]	Reserved	EXT_INT41[5]
(gpx1-4)	J3	14	XEINT_12	I	I	O	WAKEUP_INT1[4]	KP_COL[4]	Reserved	ALV_DBG[8]	Reserved	EXT_INT41[4]
(gpx1-0)	J3	16	XEINT_8	I	I	O	WAKEUP_INT1[0]	KP_COL[0]	Reserved	ALV_DBG[4]	Reserved	EXT_INT41[0]
(gpx0-7)	J3	18	DRD_VBUS_SENSE_0	I	I	O	WAKEUP_INT0[7]	Reserved	Reserved	ALV_DBG[3]	Reserved	EXT_INT40[7]
(gpx0-6)	J3	20	XEINT_6	I	I	O	WAKEUP_INT0[6]	Reserved	Reserved	ALV_DBG[2]	Reserved	EXT_INT40[6]
(gpx0-5)	J3	22	XEINT_5	I	I	O	WAKEUP_INT0[5]	Reserved	Reserved	ALV_DBG[1]	Reserved	EXT_INT40[5]
(gpx0-4)	J3	24	XEINT_4	EINT	I	O	WAKEUP_INT0[4]	Reserved	Reserved	ALV_DBG[0]	Reserved	EXT_INT40[4]
(gpx0-3)	J3	26	XEINT_3	I	I	O	WAKEUP_INT0[3]	Reserved	Reserved	Reserved	Reserved	EXT_INT40[3]
(gpx0-2)	J3	28	XEINT_2	I	I	O	WAKEUP_INT0[2]	Reserved	Reserved	Reserved	Reserved	EXT_INT40[2]
(gpx0-1)	J3	30	XEINT_1	I	I	O	WAKEUP_INT0[1]	Reserved	Reserved	Reserved	Reserved	EXT_INT40[1]
(gpx0-0)	J3	32	XEINT_0	I	I	O	WAKEUP_INT0[0]	Reserved	Reserved	Reserved	Reserved	EXT_INT40[0]
(gpx1-3)	J3	34	XGPIO17/XT_INT163	I	I	O	WAKEUP_INT1[3]	KP_COL[3]	Reserved	ALV_DBG[7]	Reserved	EXT_INT41[3]
(gpa1-4)	J3	38	Xu3_RXD	UART_3_RXD	I	O	UART_3_RXD	Reserved	Reserved	Reserved	Reserved	EXT_INT2[4]
(gpa1-5)	J3	40	Xu3_TXD	UART_3_TXD	I	O	UART_3_TXD	Reserved	Reserved	Reserved	Reserved	EXT_INT2[5]
(gpc1-4)	J3	48	XAudi2s2SDO	I	I	O	I2S_2_SDO	PCM_2_SOUT	I2C_6_SCL	Reserved	Reserved	EXT_INT5[4]
(gpc1-3)	J3	50	XAudi2s2SDI	I	I	O	I2S_2_SDI	PCM_2_SIN	I2C_6_SDA	Reserved	Reserved	EXT_INT5[3]
(gpc1-0)	J3	52	XAudi2s2SCLK	I	I	O	I2S_2_SCLK	PCM_2_SCLK	Reserved	Reserved	Reserved	EXT_INT5[0]
(gpc1-2)	J3	54	XAudi2s2LRCK	I	I	O	I2S_2_LRCK	PCM_2_FSYNC	Reserved	Reserved	Reserved	EXT_INT5[2]
(gpc1-1)	J3	56	XAudi2s2CDCLK	I	I	O	I2S_2_CDCLK	PCM_2_EXTCLK	Reserved	Reserved	Reserved	EXT_INT5[1]
(gpc0-3)	J3	60	CODEC_PDN	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT4[3]

Table 17. Type A GPIO Alternate Functions Connector J4

Connector J4 Type A GPIO												
IO Group	Conn #	Pin #	Name	Default I/O	F1	F2	F3	F4	F5	F6	F7	F8
(gpb-0)	J4	1	XspiCLK0	I	I	O	SPI_0_CLK	I2C_4_SDA	Reserved	Reserved	Reserved	EXT_INT3[0]
(gpb-1)	J4	3	XspiCSn0	I	I	O	SPI_0_nSS	I2C_4_SCL	Reserved	Reserved	Reserved	EXT_INT3[1]
(gpb-2)	J4	5	XspiMISO0	I	I	O	SPI_0_MISO	I2C_5_SDA	Reserved	Reserved	Reserved	EXT_INT3[2]
(gpb-3)	J4	7	XspiMOSI0	I	I	O	SPI_0_MOSI	I2C_5_SCL	Reserved	Reserved	Reserved	EXT_INT3[3]
(gpm0-0)	J4	9	PSR_TE	I	I	O	CAM_BAY_PCLK	CAM_B_PCLK	Reserved	TraceClk	Reserved	EXT_INT8[0]
(gpd0-2)	J4	11	Xi2c7_SDA	I	I	O	TOUT_2	I2C_7_SDA	Reserved	Reserved	Reserved	EXT_INT6[2]
(gpd0-3)	J4	13	Xi2c7_SCL	I	I	O	TOUT_3	I2C_7_SCL	Reserved	Reserved	Reserved	EXT_INT6[3]
(gpd1-3)	J4	15	Xi2c1_SCL	I	I	O	I2C_1_SCL	Reserved	Reserved	Reserved	Reserved	EXT_INT7[3]
(gpd1-2)	J4	17	Xi2c1_SDA	I	I	O	I2C_1_SDA	Reserved	Reserved	Reserved	Reserved	EXT_INT7[2]
(gpm3-2)	J4	19	VTCAM_RESET	O	I	O	CAM_GPIO[4]	MPWM5_OUT_ISP	CAM_SPI1_MISO	Reserved	Reserved	EXT_INT11[2]
(gpm4-0)	J4	21	XISP2_SCL0	I	I	O	CAM_I2C0_SCL	CAM_GPIO[10]	Reserved	Reserved	Reserved	EXT_INT12[0]
(gpm4-1)	J4	23	XISP2_SDA0	I	I	O	CAM_I2C0_SDA	CAM_GPIO[11]	Reserved	Reserved	Reserved	EXT_INT12[1]
(gpd0-1)	J4	45	Xpwmo_1	I	I	O	TOUT_1	Reserved	Reserved	Reserved	Reserved	EXT_INT6[1]
(gpd0-0)	J4	47	Xpwmo_0	I	I	O	TOUT_0	Reserved	Reserved	Reserved	Reserved	EXT_INT6[0]
(gpa1-3)	J4	53	Xi2c3_SCL	UART_2_RTSn	I	O	UART_2_RTSn	I2C_3_SCL	Reserved	Reserved	Reserved	EXT_INT2[3]
(gpa1-2)	J4	55	Xi2c3_SDA	UART_2_CTSn	I	O	UART_2_CTSn	I2C_3_SDA	Reserved	Reserved	Reserved	EXT_INT2[2]
(gpe2-1)	J4	57	LCD_RST	O	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe0-3)	J4	59	XGPIO3	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
(gpm4-4)	J4	12	GPM4_4	I	I	O	CAM_SPI_CLK	CAM_GPIO[14]	Reserved	Reserved	Reserved	EXT_INT12[4]
(gpm4-5)	J4	14	GPM4_5	I	I	O	CAM_SPI_nSS	CAM_GPIO[15]	Reserved	Reserved	Reserved	EXT_INT12[5]
(gpm4-6)	J4	16	GPM4_6	I	I	O	CAM_SPI_MISO	CAM_GPIO[16]	Reserved	Reserved	Reserved	EXT_INT12[6]
(gpm4-7)	J4	18	GPM4_7	I	I	O	CAM_SPI_MOSI	CAM_GPIO[17]	Reserved	Reserved	Reserved	EXT_INT12[7]
(gpc0-4)	J4	56	GPC0_4	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT4[4]
(gpe0-2)	J4	60	XGPIO2	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 18. Type B GPIO Alternate Functions Connector J4

Connector J4 Type B GPIO												
IO Group	Conn #	Pin #	Name	Default I/O	F1	F2	F3	F4	F5	F6	F7	F8
(gpk2-2)	J4	40	XMMC2CDN	I		I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpk2-0)	J4	42	XMMC2CLK	O		I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpk2-1)	J4	44	XMMC2CMD	O		I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpk2-3)	J4	46	XMMC2DATA0	I		I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpk2-4)	J4	48	XMMC2DATA1	I		I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpk2-5)	J4	50	XMMC2DATA2	I		I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpk2-6)	J4	52	XMMC2DATA3	I		I	O	Reserved	Reserved	Reserved	Reserved	Reserved

Table 19. Type A GPIO Alternate Functions Connector J5

Connector J5 Type A GPIO												
IO Group	Conn #	Pin #	Name	Default I/O	F1	F2	F3	F4	F5	F6	F7	F8
(gpe0-4)	J5	3	EBI_OEn	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe0-5)	J5	5	EBI_Wen	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe0-1)	J5	7	EBI_CSn	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe0-7)	J5	11	EBI_ADDR0	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe1-0)	J5	13	EBI_ADDR1	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe1-1)	J5	15	EBI_ADDR2	I	O	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe1-2)	J5	17	EBI_ADDR3	I	O	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe1-3)	J5	19	EBI_ADDR4	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe1-4)	J5	21	EBI_ADDR5	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpe1-5)	J5	23	EBI_ADDR6	I	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved
(gpm0-4)	J5	27	EBI_DAT0	I	O	I	O	CAM_BAY_RGB[3]	CAM_B_DATA[3]	Reserved	TraceData[3]	Reserved
(gpm0-5)	J5	29	EBI_DAT1	I	I	I	O	CAM_BAY_RGB[4]	CAM_B_DATA[4]	Reserved	TraceData[4]	Reserved
(gpm0-6)	J5	31	EBI_DAT2	I	I	I	O	CAM_BAY_RGB[5]	CAM_B_DATA[5]	Reserved	TraceData[5]	Reserved
(gpm0-7)	J5	33	EBI_DAT3	I	I	I	O	CAM_BAY_RGB[6]	CAM_B_DATA[6]	Reserved	TraceData[6]	Reserved
(gpm1-0)	J5	35	EBI_DAT4	I	I	I	O	CAM_BAY_RGB[7]	CAM_B_DATA[7]	Reserved	TraceData[7]	Reserved
(gpm1-1)	J5	37	EBI_DAT5	I	I	I	O	CAM_BAY_RGB[8]	CAM_B_FIELD	Reserved	TraceCtl	Reserved
(gpm1-2)	J5	39	EBI_DAT6	I	I	I	O	CAM_BAY_RGB[9]	Reserved	Reserved	TraceData[8]	Reserved
(gpm1-3)	J5	41	EBI_DAT7	I	I	I	O	CAM_BAY_RGB[10]	Reserved	Reserved	TraceData[9]	Reserved
(gpm1-4)	J5	43	EBI_DAT8	I	I	I	O	CAM_BAY_RGB[11]	Reserved	Reserved	TraceData[10]	Reserved
(gpm1-5)	J5	45	EBI_DAT9	I	I	I	O	CAM_BAY_RGB[12]	Reserved	Reserved	TraceData[11]	Reserved
(gpm1-6)	J5	47	EBI_DAT10	I	I	I	O	CAM_BAY_RGB[13]	Reserved	Reserved	TraceData[12]	Reserved
(gpm2-0)	J5	49	EBI_DAT11	I	I	I	O	CAM_BAY_Vsync	CAM_B_VSYNC	Reserved	TraceData[13]	Reserved
(gpm2-1)	J5	51	EBI_DAT12	I	I	I	O	CAM_BAY_Hsync	CAM_B_HREF	Reserved	TraceData[14]	Reserved
(gpm2-2)	J5	53	EBI_DAT13	I	I	I	O	CAM_BAY_MCLK	CAM_B_CLKOUT	Reserved	TraceData[15]	Reserved
(gpm2-3)	J5	55	EBI_DAT14	I	I	I	O	CAM_GPIO[0]	MPWM1_OUT_ISP	Reserved	Reserved	Reserved
(gpm2-4)	J5	57	EBI_DAT15	I	I	I	O	CAM_GPIO[1]	MPWM2_OUT_ISP	Reserved	Reserved	Reserved
(gpm3-1)	J5	4	GPM3_1	I	I	I	O	CAM_GPIO[3]	MPWM4_OUT_ISP	Reserved	Reserved	Reserved
(gpm3-0)	J5	6	GPM3_0	I	I	I	O	CAM_GPIO[2]	MPWM3_OUT_ISP	Reserved	Reserved	Reserved
(gpa1-0)	J5	26	DEBUG_RXD	I	UART_2_RXD	I	O	UART_2_RXD	Reserved	Reserved	Reserved	Reserved
(gpa1-1)	J5	28	DEBUG_TXD	I	UART_2_TXD	I	O	UART_2_TXD	Reserved	Reserved	Reserved	Reserved

ARTIK 520 Module Booting Sequence

During system reset, the program that is stored in iROM (internal ROM), that is part of the ARTIK 520 Module, is executed from address 0x0000_0000. The iROM area is, by default, mapped to this address. The system reset may be asserted during the time of booting and wake-up by using low-power modes. As a consequence, the boot loader executes appropriate processes according to the reset status. There are two boot loaders to initiate a first and a second boot, implemented according to a typical bootstrap loading procedure.

Typically, there are four steps in the ARTIK 520 Module booting process:

1. After reset, the iROM code that contains a small program to initialize the processor system is executed. The iROM is an internal 64 KB ROM, it initializes basic system functions such as Clock and Stack and it initializes the SD/MMC controller. The iROM code is also responsible for loading the Boot Loader 1 (BL1) image from an external memory device to the internal SRAM (iSRAM). The iROM code verifies the BL1 image, to assure that the image is authentic and that the calculated hash is associated with the preset secure boot key. As a last step, the iROM code jumps to the start of the BL1 code so that execution of the BL1 code can start.
2. The BL1 is still a processor system specific boot. The BL1 code that was transferred to the local iSRAM using the iROM executable is now executed and it will start initializing the system clocks and the DRAM controller. Now the BL2 code can be loaded into DRAM and executed from there. As a last step, the BL1 code will jump to the start of the BL2 code so that execution of the BL2 code can start from DRAM.
3. The BL2 will now load the OS into DRAM and control will be transferred to the OS.
4. The OS has started upon completion of the boot process and can load a specific IoT application that will, as part of its function, initialize Bluetooth, ZigBee etc., before it executes its specific IoT task.

The type of booting can be determined by changing the levels of two pins on Connector J3:[35,37].*Table 20* provides the two booting options that are available. If the first device choice does not work to boot up the ARTIK 520 Module, the second device choice will be tried automatically.

Table 20. Booting Options

BOOT Con#:[Pin#]	Bit:[xx]	First Device	Second Device
J3:[37,35]	2b'01	SD/MMC	USB
	2b'10	eMMC	USB

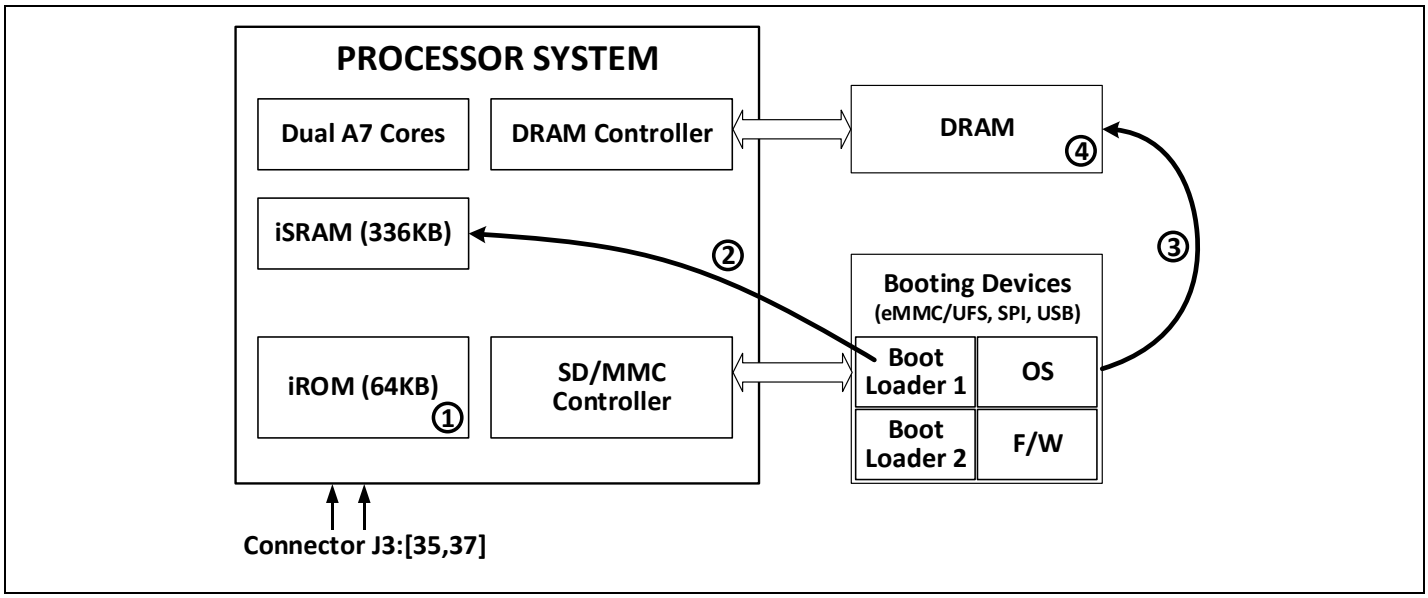

Figure 5. ARTIK 520 Module Booting Sequence

ARTIK 520 Module Reset Scenarios

There are 5 different reset scenarios that are supported on the ARTIK 520 Module:

- Hardware reset
- Watchdog reset
- Software reset
- Wake up from SLEEP
- Wake up from DEEP-STOP

Table 21 lists the mandatory functions that will be executed per reset scenario.

Table 21. Required Functions per Reset Type

Reset Type	Initialization in iROM	PLL Setting in iROM	BL1 Execution	PLL and DRAM Setting in BL1	OS Loading	Restore Previous State
Hardware Reset	–	–	–	–	–	X
Watchdog Reset	–	–	–	–	–	X
Software Reset	–	–	–	–	–	X
Wake up from SLEEP	–	–	–	–	X	–
Wake up from DEEP-STOP	–	X(1)	X	–	X	–
Wake up from Low Power Audio (LPA)	–	X(1)	X	–	X	–

1. During software reset, the contents of the internal SRAM and the external DRAM are preserved. However, when waking up from a DEEP-STOP, BL1, BL2 and the OS must be loaded to ensure software integrity. SRAM is preserved in this mode and as such it is not required to reload the boot loader.

Note: X means action will take place after particular Reset Type.

For more information on how to implement various reset strategies, please consult the ARTIK 520 Module SW Developer's Guide.

ARTIK 520 Module Antenna Connections

Two antennas are required to use the full set of radio communication links on the ARTIK 520 Module. One supports the combination of Wi-Fi and BT, and the other is dedicated to ZigBee.

Caution: Do not apply power (enable) the radio chips before connecting antennas or damage to the chip may result.

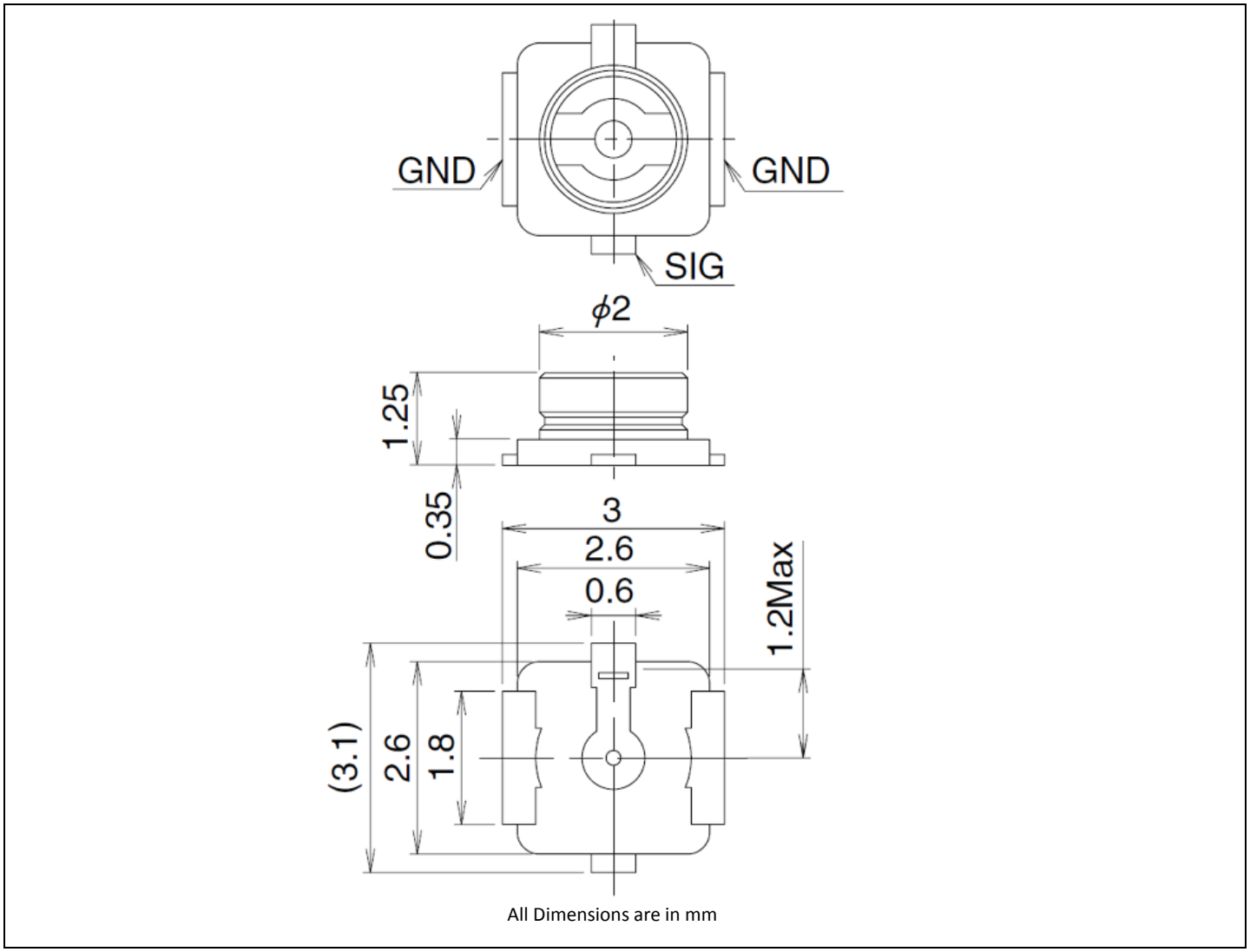

Figure 6. Hirose RF Connector for BT/Wi-Fi and ZigBee

The U.FL-R-SMT Hirose connector is used for both the BT/Wi-Fi and the ZigBee antenna connectors on the ARTIK 520 Module.

The mechanical size of the connector (receptacle) is described in *Figure 6*. For suggestions on mating plug and more details on the connector, please contact Hirose Electric Co., LTD.

ARTIK 520 Module Electrical Specifications

Absolute Maximum Ratings

The ratings given in this section are associated only with stress. It does not imply any functional operation of the device. Exposure to the absolute-maximum rated conditions for long duration affects the reliability of the device.

Table 22. Absolute Maximum Ratings

Absolute Maximum Ratings					
Parameter	**Symbol**		**Min.**	**Max.**	**Units**
Main battery supply	MAIN_BAT		-0.3	6.0	V
DC input/output voltage	**Type A IO:** J3:[9,11,13,15,17,19,21,23,25,27,29,39,41,43,45,47,49,57,59,12,14,16,18,20,22,24,26,28,30,32,34,38,40,48,50,52,54,56,60] J4:[1,3,5,7,9,11,13,15,17,19,21,23,45,47,53,55,57,59,12,14,16,18,56,60] J5:[3,5,7,11,13,15,17,19,21,23,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,4,6,26,28]	1.8V Input Buffer	-0.5	2.5	
	Type B IO: J3:[18,20,22,24,26,28,30,32] J4:[40,42,44,46,48,50,52]	3.3V Input Buffer	-0.5	3.8	
DC input/output voltage	**ZIGBEE** J5:[46,48,50,52,54,56,58,60]	2.80V Input/output buffer	-0.3	3.1	
Input output current	**Type A, Type B IO current** J3:[9,11,13,15,17,19,21,23,25,27,29,39,41,43,45,47,49,57,59,12,14,16,18,20,22,24,26,28,30,32,34,38,40,48,50,52,54,56,60] J4:[1,3,5,7,9,11,13,15,17,19,21,23,45,47,53,55,57,59,12,14,16,18,40,42,44,46,48,50,52,56,60] J5:[3,5,7,11,13,15,17,19,21,23,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,4,6,26,28]		±20		mA
Storage Temperature	T_A		-40 to 125		°C

Recommended Operating Conditions

The recommended operation of the ARTIK 520 Module is based on the operating conditions listed in *Table 23*.

Table 23. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Main Battery Supply	MAIN_BAT J3:[1,3,2,4]	3.13	3.80	4.80	V
Operating Temperature	T_O	-25	–	85	°C

DC Module Use Case Characteristics

Power Supply Requirements

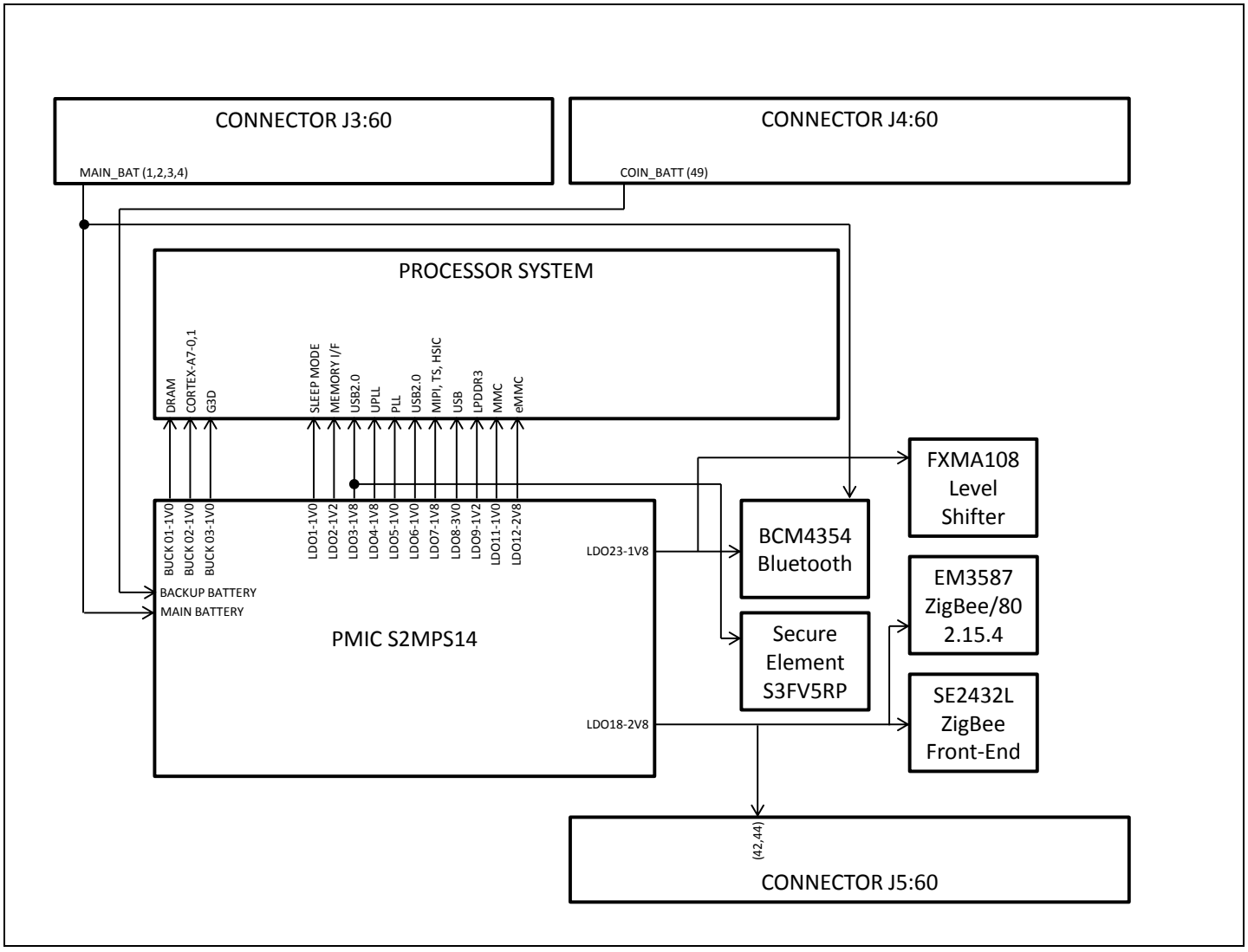

Figure 7. ARTIK 520 Module Power Distribution

The power management of the ARTIK 520 Module as described in *Figure 7* is controlled by the Samsung PMIC (S2MPS14). This PMIC contains 5 Bucks and 25 LDO Regulators. See *Table 24* and *Table 25* for details on voltage and amperage ranges and how they are used in the ARTIK 520 Module.

Table 24. Buck Description and Default Setting

Buck Number	Pin	Powers	Current [mA]	Range [V]	Step [mV]	Default [V]
1	Buck01	Processor System:[MIF]	300	0.65-1.60	6.25	1.00
2	Buck02	Processor System:[CORTEX®]	1000	0.65-1.60	6.25	1.00
3	Buck03	Processor System:[G3D]	700	0.65-1.60	6.25	1.00
4	Buck04	–	–	–	–	–
5	Buck05	–	–	–	–	–

Table 25. PMIC LDOs

LDO Number	Pin	Powers	Current [mA]	Range [V]	Step [mV]	Default [V]
1-N	LDO1	Processor System:[ALIVE]	150	0.900-1.100	12.5	1.00
2-N	LDO2	Processor System:[Memory Interface]	150	1.075-1.400	12.5	1.20
3-P	LDO3	Processor System:[LPDDR3 core]	300	1.600-2.000	25	1.80
4-P	LDO4	Processor System:[UPLL]	150	1.600-2.000	25	1.80
5-N	LDO5	Processor System:[PLL]	150	0.900-1.212	12.5	1.00
6-N	LDO6	Processor System:[USB]	150	0.900-1.212	12.5	1.00
7-P	LDO7	Processor System:[MIPI, TS, HSIC]	150	1.600-2.000	25	1.80
8-P	LDO8	Processor System:[USB]	150	2.250-3.300	25	3.00
9-N	LDO9	Processor System:[LPDDR3]	300	1.075-1.500	12.5	1.20
10-N	LDO10	–	150	0.900-1.100	12.5	1.00
11-P	LDO11	Processor System:[eMMC]	150	0.800-2.375	25	1.80
12-P	LDO12	Processor System:[eMMC]	150	1.800-3.375	25	2.80
13-P	LDO13	–	150	1.800-3.375	25	2.80
14-P	LDO14	–	150	1.800-3.375	25	2.70
15-P	LDO15	–	150	1.800-3.375	25	3.30
16-P	LDO16	–	150	1.800-3.375	25	3.30
17-P	LDO17	–	300	1.800-3.375	25	3.00
18-P	LDO18	J5:[42,44] ZigBee	300	1.800-3.375	25	2.80
19-P	LDO19	–	300	0.800-2.375	25	1.80
20-P	LDO20	–	150	0.800-2.375	25	1.80
21-P	LDO21	–	150	0.800-2.375	25	1.25
22-N	LDO22	–	150	0.800-1.500	12.5	1.20
23-P	LDO23	FXMA108, BCM4354	150	0.800-2.375	25	1.80
24-P	LDO24	–	150	1.800-3.375	25	3.00
25-P	LDO25	–	150	1.800-3.375	25	3.00

Table 26. AC/DC Characteristics LDO18

LDO 18, Connector J5:[42,44], MAIN_BAT=3.8V, T_A=25°C unless otherwise specified						
Characteristics	**Test Conditions**		**Min**	**Typ**	**Max**	**Unit**
Input voltage range (V_{INL})	–		1.80	(V_{LDO}+0.2)*	MAIN_BAT	V
Output voltage range	I_L=300mA programmable 25mV steps		1.80	–	3.375	V
Default output voltage	300mA@V_{INL}=V_{LDO}+0.2V		–	2.80	–	V
Maximum load current	Normal mode		300	–	–	mA
	Low power mode		5	–	–	mA
Output current limit	V_{OUT}=90% of V_{LDO}		330	480	900	mA
Minimum output bypass capacitance	–		2.2	–	–	µF
Ground Current	Battery supply current no load	Shutdown	–	< 0.1	–	µA
		Normal regulation	–	18	30	
		Low power mode	–	3.5	6	
Output voltage accuracy	Normal mode V_{INL} = V_{LDO}+0.2V to MAIN_BAT, I_L=0.1mA-300mA		-3	–	+3	%
	Low power mode V_{INL}=V_{LDO}+0.2V to MAIN_BAT, I_L = 0.1mA-5mA		-3	–	+3	
Load Regulation	Normal mode V_{INL} = V_{LDO}+0.2V to MAIN_BAT, I_L=0.1mA-300mA		–	0.1	–	%
	Low power mode V_{INL}=V_{LDO}+0.2V MAIN_BAT=V_{LDO}+1.5V, I_L = 0.1mA-5mA		–	0.2	–	
Line Regulation	Normal mode V_{INL} = V_{LDO}+0.2V to MAIN_BAT, I_L=0.1mA		–	0.05	–	%/V
	Low power mode V_{INL}=V_{LDO}+0.2V,I_L = 0.1mA		–	0.1	–	
Drop-out voltage	Normal mode V_{LDO}=3.3V, I_L=300mA		–	60	120	mV
	Normal mode V_{LDO}=1.8V, I_L=300mA		–	100	200	
	Low power mode V_{LDO}=3.3V, I_L=5mA		–	150	300	
Output load transient	Normal mode, V_{INL}=V_{LDO}+0.2V, I_L=3mA-300mA, and vice versa, t_r=t_f=10µs		–	60	90	mV
Output line transient	Normal Mode V_{INL}=V_{LDO}+0.2V to V_{LDO}+0.7V and vice versa, t_r=t_f=1µs, I_L=300mA		–	10	20	mV
Power Supply Rejection Ratio (PSRR)	f=1kHz to 10KHz, I_L=30mA, V_{INL}=VLDO+0.2V+50mV_{pp}	1kHz	–	70	–	dB
		10kHz	–	50	–	
Output Noise	f=10Hz-100kHz,C_L=2.2 µF, I_L=30mA	V_{LDO}=1.8V V_{INL}=V_{LDO}+0.2V	–	60	–	µVrms
		V_{LDO}=3.3V V_{INL}=V_{LDO}+0.2V	–	80	–	
Soft Start Time	0 to 90% settling time		–	30	100	µs
Disable Delay (t_{off})	After LDO is disabled; The LDO output voltage will discharge based on load current (I_L) and C_L		–	0.1	–	µs
Active Discharge Resistance	Output Disabled		0.05	0.1	0.2	kΩ
Clamp Active Regulation Voltage	Current Sink up to 5mA for VLDO Clamping		V_{LDO}+0.5%	–	V_{LDO}+4%	V
Thermal shutdown	Tj rising		–	165	–	°C
	Tj falling		–	150	–	

*By default V_{LDO} is set to 2.8V to assure that ZigBee operates optimally, however you can program V_{LDO} between 1.80 and 3.175 to assure ZigBee functionality. See the respective vendor datasheets and the software developers guide for more details.

ESD Ratings

Table 27. ESD Ratings

Symbol	Min.	Max.	Units
ESD stress voltage Human Body Model	–	1	kV
ESD stress voltage Charged Device Model	–	250	V

Table 28. Shock and Vibration Ratings

Shock and Vibration		Range
Shock	Operating	TBD
	Non Operating	TBD
Vibration	Operating	TBD
	Non Operating	TBD

DC Electrical Characteristics

The entire DC characteristics are listed in *Table 29*. For each pin input sense levels, output drive levels, and currents are included. Use these parameters to determine maximum DC loading and to determine maximum transition times for a given load. *Table 29* shows the DC operating conditions for the high- and low-strength input, output and I/O pins.

Table 29. I/O DC Electrical Characteristics

V_{DD} = 1.8V, V_{ext} = 3.0 to 3.6 V, T_j = -40 to 85 °C (Junction Temperature)

GPIO Con#:[Pin#]	Parameter		Condition		Min.	Typ.	Max.	Units
Type A/B IO (1V8): J3:[9,11,13,15,17,19,21, 23,25,27,29,39,41,43,45, 47,49,57,59,12,14,16,18, 20,22,24,26,28,30,32,34, 38,40,48,50,52,54,56,60] J4:[1,3,5,7,9,11,13,15,17, 19,21,23,45,47,53,55,57, 59,12,14,16,18,40,42,44, 46,48,50,52,56,60] J5:[3,5,7,11,13,15,17,19, 21,23,27,29,31,33,35,37, 39,41,43,45,47,49,51,53, 55,57,4,6,26,28]	Vtol	Tolerant external voltage	V_{DD} Power Off & On		–	–	3.60	V
	V_{IH}	**High Level Input Voltage**						
		CMOS Interface	–		07xV_{DD}	–	V_{DD}+0.3	V
	V_{IL}	**Low Level Input Voltage**						
		CMOS Interface	V_{DD} = 1.8V ± 10 %		-0.3	–	0.54	V
	ΔV	Hysteresis Voltage	–		0.15	–		V
	I_{IH}	**High Level Input Current**						
		Input Buffer	V_{IN} = V_{DD}	V_{DD} Power On	-3	–	3	µA
				V_{DD} Power Off & SNS = 0	-5	–	5	
		Input Buffer with pull-down	V_{IN} = V_{DD}	V_{DD} = 1.8V ± 10 %	20	40	80	
	I_{IL}	**Low Level Input Current**						
		Input Buffer	V_{IN} = V_{SS}	V_{DD} Power On & Off	-3	–	3	µA
		Input Buffer with pull-up	V_{IN} = V_{SS}	V_{DD} = 1.8V ± 10 %	-15	-40	-80	
	V_{OH}	Output High Voltage	I_{OH} = -1.8mA, -3.8mA, -1.8mA, -11mA		1.44	–	V_{DD}	V
	V_{OL}	Output Low Voltage	I_{OL} = 1.8mA, 3.8mA, 1.8mA, 11mA		0	–	0.36	
	I_{OZ}	Output Hi-Z current			-5	–	5	µA
	C_{IN}	Input capacitance	Any input and bi-directional buffers		–	–	5	pF

Note:

1. The values of I_{OH} and I_{OL} are valid only for 3.3 V range.
2. The value of I_{OH} and I_{OL} is for min. driver strength.

Table 30. I/O DC Electrical Characteristics ZIGBEE

ZIGBEE Con#:[Pin#]	Parameter	Test Condition	Min.	Typ.	Max.	Units
J5:[46,48,50,54,56,58,60]	Low Schmitt switching threshold	V_{SWIL} Schmitt input threshold going from high to low	1.18	–	1.40	V
	High Schmitt switching threshold	V_{SWIH} Schmitt input threshold going from low to high	1.74	–	2.24	V
	Input current for logic 0	I_{IL}	–	–	-0.5	µA
	Input current for logic 1	I_{IH}	–	–	+0.5	µA
	Input pull-up resistor value	R_{IPU}	24	29	34	kΩ
	Input pull-down resistor value	R_{IPD}	24	29	34	kΩ
	Output voltage for logic 0	V_{OL} (I_{OL} = 4mA for standard pads, 8mA for high current pads)	0	–	0.50	V
	Output voltage for logic 1	V_{OH} (I_{OH} = 4mA for standard pads, 8mA for high current pads)	2.30	–	2.80	V
	Output source current (standard current pad)	I_{OHS}	–	–	4	mA
	Output sink current (standard current pad)	I_{OLS}	–	–	4	mA
	Output source current high current pad: J5:[48]	I_{OHH}	–	–	8	mA
	Output sink current high current pad: J5:[48]	I_{OLH}	–	–	8	mA
	Total output current (for I/O Pads)	I_{OH} + I_{OL}	–	–	40	mA

Table 31. I/O DC Electrical Characteristics PMIC

PMIC Con#:[Pin#]	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
J3:[10]	Power on key input	PWRON	–	1.40	–	–	V
	Pull down input resistor, internally connected to AGND			–	800	–	kΩ

Table 32. I/O DC Electrical Characteristics USB

USB Con#:[Pin#]	Parameter	Symbol	Condition	Min.	Max.	Unit
J4:[2,4,8,10]	High level input voltage	V_{IH}	–	2.0	–	V
	Low level input voltage	V_{IL}	–	–	0.8	
	High level input current	I_{IH}	Vin = 3.3 V	-10	10	µA
	Low level input current	I_{IL}	Vin = 0.0 V	-10	10	
	Static Output High	V_{OH}	14.25 kΩ to GND	2.8	3.6	V
	Static Output Low	V_{OL}	1.425 kΩ to 3.6 V		0.3	
	Valid level voltage	V_{BUS}		4.4	5.25	

IO Driver Strength Tables

The driver strength characteristics for the various I/Os operating at 1V8 available on Connectors J3, J4 and J5 are given in *Table 33* and *Table 34*.

Type A I/O Driver Strength

Table 33. Type A I/O Driver Strength and Delay Time

GPIO Con#:[Pin#]	Input DS		Output PAD (Driving Strength)	Output PAD (Slew Rate)	
				CL=5pF	CL=10pF
J3:[9,11,13,15,17,19,21,23,25,27,29,39,41,43,45,47,49,57,59,12,14,16, 18,20,22,24,26,28,30,32,34,38,40,48,50,52,54,56,60] J4:[1,3,5,7,9,11,13,15,17,19,21,23,45,47,53,55,57,59,12,14,16,18,56,60] J5:[3,5,7,11,13,15,17,19,21,23,27,29,31,33,35,37,39,41,43,45,47,49,51, 53,55,57,4,6,26,28]	0	0	2mA	1.9ns	2.5ns
	0	1	4mA	2.7ns	2.7ns
	1	0	8mA	1.1ns	1.2ns
	1	1	12mA	0.9ns	1.1ns

Table 34. Type A I/O Pull-up/Down Resistor

GPIO Con#:[Pin#]	V_{DD}=1.8V	Worst V_{DD}=1.65V T=125°C, Process=Slow	Worst V_{DD}=1.95V T=-40°C, Process=Fast
J3:[9,11,13,15,17,19,21,23,25,27,29,39,41,43,45,47,49,57,59,12,14,16, 18,20,22,24,26,28,30,32,34,38,40,48,50,52,54,56,60]	Pull-up	45kΩ	13kΩ
J4:[1,3,5,7,9,11,13,15,17,19,21,23,45,47,53,55,57,59,12,14,16,18,56,60] J5:[3,5,7,11,13,15,17,19,21,23,27,29,31,33,35,37,39,41,43,45,47,49,51, 53,55,57,4,6,26,28]	Pull-down	45kΩ	15kΩ

Type B I/O Driver Strength

The driver strength characteristics for the various I/Os operating at 3V3 available on Connector J4 are given in *Table 35* and *Table 36*.

Table 35. Type B I/O Output Cell Delay Time

GPIO Con#:[Pin#]	Input DS		Output PAD (Driving Capability)	Output PAD (Slew Rate)	
				CL=5pF	CL=10pF
J4:[40,42,44,46,48,50,52]	0	0	x1	2.5ns	3.2ns
	0	1	x2	1.8ns	2.2ns
	1	0	x3	1.4ns	1.6ns
	1	1	x4	1.3ns	1.5ns

Table 36. Type B I/O Pull Up/Down Controller

GPIO Con#:[Pin#]	V_{DD}=3.3V±0.3V	Worst V_{DD}=3.00V T=125°C, Process=Slow	Typical V_{DD}=3.30V T=25°C, Process=Typical	Worst V_{DD}=3.60V T=-40°C, Process=Fast
J4:[40,42,44,46,48,50,52]	Pull-up	135kΩ	85kΩ	37kΩ
	Pull-down	165kΩ	80kΩ	44kΩ
	VDD=2.5V±0.2V	Worst VDD=2.30V T=125°C, Process=Slow	Typical VDD=2.50V T=25°C, Process=Typical	Worst VDD=2.70V T=-40°C, Process=Fast
	Pull-up	140kΩ	68kΩ	25kΩ
	Pull-down	125kΩ	65kΩ	34kΩ
	VDD=1.8V±0.15V	Worst VDD=1.65V T=125°C, Process=Slow	Typical VDD=1.80V T=25°C, Process=Typical	Worst VDD=1.95V T=-40°C, Process=Fast
	Pull-up	80kΩ	48kΩ	30kΩ
	Pull-down	80kΩ	48kΩ	30kΩ

Table 37. Power on Reset Timing Specifications

(V_{DDINT}= 1.1V ± 5%, T_A = –25 to 85°C, V_{DDSYS} = 3.3V ± 5 %, 2.5V ± 0.25V, 1.8V ± 0.15V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RESW}	Reset assert time after clock stabilization	167	–	–	ns

AC Electrical Characteristics

SDMMC AC Electrical Characteristics

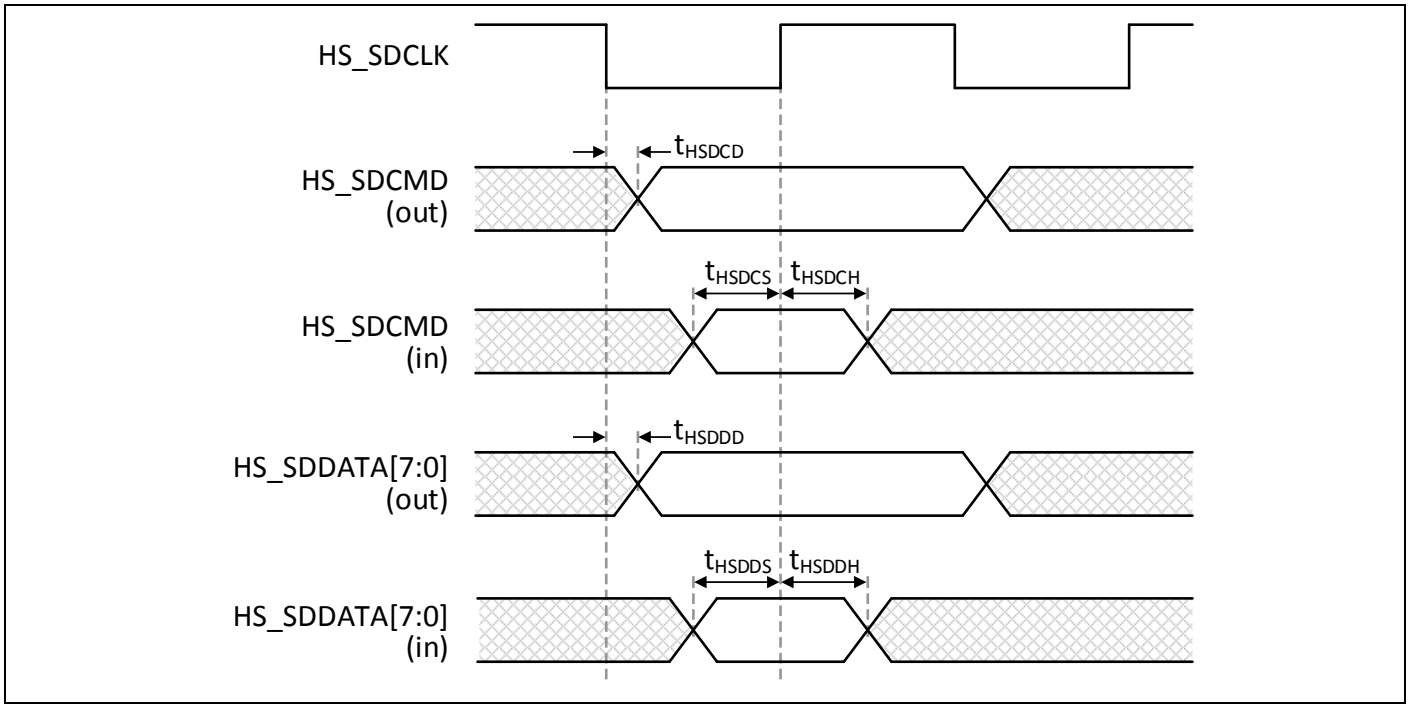

Figure 8. High Speed SDMMC Interface Timing

Table 38. High Speed SDMMC Interface Transmit/Receive Timing Constants

(V_{DDINT} = 1.0V ± 5%, T_A = -25 to 85°C, V_{DDmmc} = 3.3V ± 5 %, 2.5V ± 5%, 1.8V ± 5%)

Connector J4:[42,44,46,48,50,52,54]					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{SDCD}	SD command output delay time	–	–	4.0	ns
t_{SDCS}	SD command input setup time	4.0	–	–	
t_{SDCH}	SD command input hold time	0	–	–	
t_{SDDD}	SD data output delay time	–	–	4.0	
t_{SDDS}	SD data input setup time	4.0	–	–	
t_{SDDH}	SD data input hold time	0	–	–	

SPI AC Electrical Characteristics

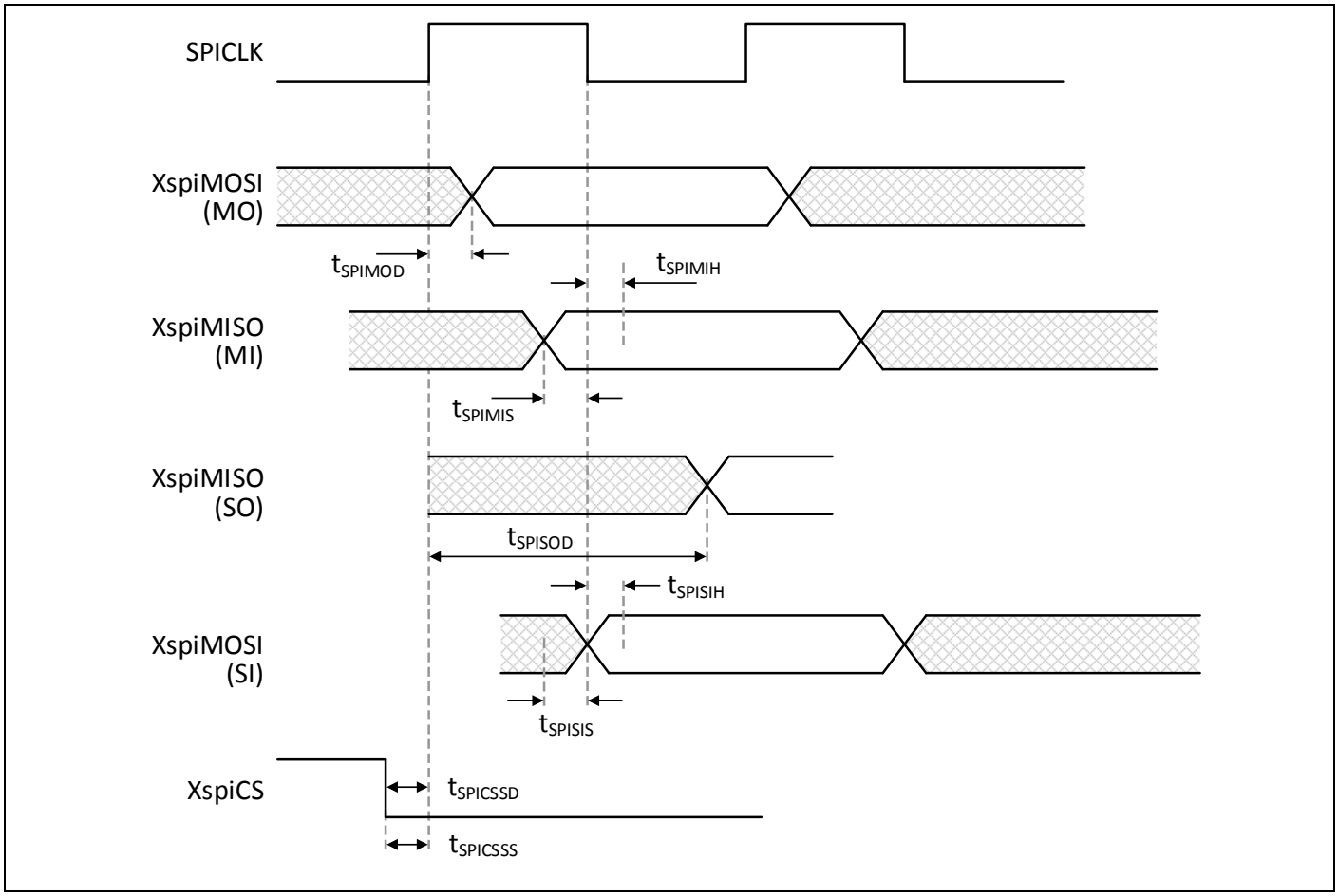

Figure 9. SPI Interface Timing (CPHA = 0, CPOL = 1 (Format A))

Table 39. SPI Interface Transmit/ Receive Timing Constants with 15pF Load

(V_{DDINT} = 1.0 V ± 5 %, T_A = -25 to 85 °C, V_{DDext} = 1.8 V ± 10 %, load = 15 pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	12	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		7	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		2	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-3	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	2	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	17	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	4	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	3	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	

Note: SPICLKout = 50 MHz

- t_{SPIMIS},CH0 = 12 – (cycle period/4) x FB_CLK_SEL
- t_{SPIMIS},CH1 = 13 – (cycle period/4) x FB_CLK_SEL

Table 40. SPI Interface Transmit/ Receive Timing Constants with 30pF Load

(VDDINT = 1.0 V ± 5 %, TA = –25 to 85 °C, VDDext = 3.3 V ± 10 %, load = 30 pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	6	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	14	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		9	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		4	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-1	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	19	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	–	–	

Note: SPICLKout = 50 MHz

- tSPIMIS,CH0 = 12 – (cycle period/4) x FB_CLK_SEL
- tSPIMIS,CH1 = 13 – (cycle period/4) x FB_CLK_SEL

I²C AC Electrical Characteristics

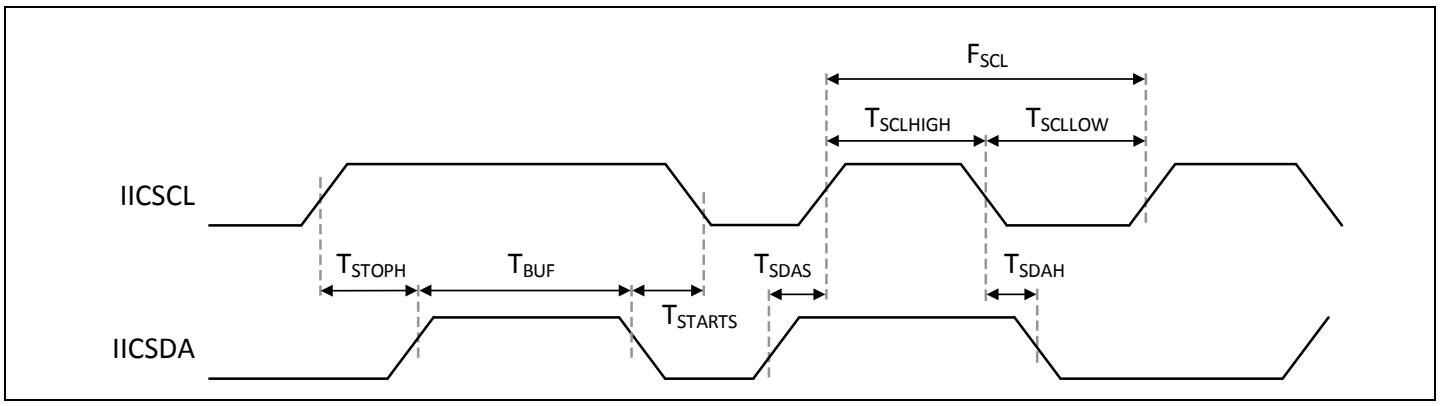

Figure 10. I²C Interface Timing

Table 41. I²C BUS Controller Module Signal Timing

(VDDINT, VDDarm = 1.1 V ± 5 %, T_A = -25 to 85 °C, VDDext = 3.3 V ± 10 %)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	F_{SCL}	–	–	std. 100 fast 400	kHz
SCL high level pulse width	$T_{SCLHIGH}$	std. 4.0 fast 0.6	–	–	µs
SCL low level pulse width	T_{SCLLOW}	std. 4.7 fast 1.3	–	–	
Bus free time between STOP and START	T_{BUF}	std 4.7 fast 1.3	–	–	
START hold time	T_{STARTS}	std. 4.0 fast 0.6	–	–	
SDA hold time	T_{SDAH}	std. 0 fast 0	–	std. fast 0.9	
SDA setup time	T_{SDAS}	std. 250 fast 100	–	–	ns
STOP setup time	T_{STOPH}	std. 4.0 fast 0.6	–	–	µs

Note: std. refers to Standard Mode and fast refers to Fast Mode.

1. The I²C data hold time (t_{SDAH}) is minimum 0ns.
   (I²C data hold time is minimum 0ns for standard/fast bus mode I²C specification v2.1)
   Check whether the data hold time of your I²C device is 0 ns or not.
2. The I²C controller supports I²C bus device only (standard/fast bus mode), and does not support C bus device.

RF Electrical Characteristics

All performance numbers related to Wi-Fi, Bluetooth and ZigBee mentioned in this section are preliminary and likely to change once module characterization has taken place.

Wi-Fi WLAN 2.4GHz Receiver RF Specifications

Table 42. Wi-Fi WLAN 2.4GHz Receiver RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Minimum receiver sensitivity in 802.11b mode					
1Mbps	PER < 8%, Packet size = 1024 bytes	–	–	-80	dBm
2Mbps		–	–	-80	dBm
5.5Mbps		–	–	-76	dBm
11Mbps		–	–	-76	dBm
Minimum receiver sensitivity in 802.11g mode					
6Mbps	PER < 10%, Packet size= 1024 bytes	–	–	-82	dBm
9Mbps		–	–	-81	dBm
12Mbps		–	–	-79	dBm
18Mbps		–	–	-77	dBm
24Mbps		–	–	-74	dBm
36Mbps		–	–	-70	dBm
48Mbps		–	–	-66	dBm
54Mbps		–	–	-65	dBm
Minimum receiver sensitivity in 802.11n mode					
MCS 0	PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC	–	–	-82	dBm
MCS 1		–	–	-79	dBm
MCS 2		–	–	-77	dBm
MCS 3		–	–	-74	dBm
MCS 4		–	–	-70	dBm
MCS 5		–	–	-68	dBm
MCS 6		–	–	-65	dBm
MCS 7		–	–	-64	dBm
Minimum receiver sensitivity in 802.11ac mode (VHT20)					
MCS 0	PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC	–	–	-82	dBm
MCS 1		–	–	-79	dBm
MCS 2		–	–	-77	dBm
MCS 3		–	–	-74	dBm
MCS 4		–	–	-70	dBm
MCS 5		–	–	-66	dBm
MCS 6		–	–	-65	dBm
MCS 7		–	–	-64	dBm
MCS 8		–	–	-59	dBm
Maximum input level					
Maximum input signal level in 802.11b mode	PER < 8%	-10	–	–	dBm
Maximum input signal level in 802.11g mode	PER < 10%	-20	–	–	dBm
Maximum input signal level in 802.11n mode	PER < 10%	-20	–	–	dBm

Parameter	Conditions	Min	Typ.	Max	Unit
Maximum input signal level in 802.11ac mode	PER < 10%	-30	–	–	dBm

Wi-Fi WLAN 2.4GHz Transmitter RF Specifications

Table 43. Wi-Fi WLAN 2.4GHz Transmitter RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Linear output power					
Maximum output power in 802.11b mode	As specified in IEEE802.11	–	19	–	dBm
Maximum output power in 802.11g mode		–	16	–	dBm
Maximum output power in 802.11n mode	HT20	–	15	–	dBm
Maximum output power in 802.11ac mode	VHT20	–	15	–	dBm
Transmit spectrum mask					
Margin to 802.11b spectrum mask	Maximum output power	0	–	–	dBr
Margin to 802.11g spectrum mask		0	–	–	dBr
Margin to 802.11n spectrum mask		0	–	–	dBr
Transmit modulation accuracy in 802.11b mode					
1Mbps	As specified in IEEE 802.11b	–	–	35	%
2Mbps		–	–	35	%
5.5Mbps		–	–	35	%
11Mbps		–	–	35	%
Transmit modulation accuracy in 802.11g mode					
6Mbps	Mandatory	–	–	-5	dB
9Mbps	Optional	–	–	-8	dB
12Mbps	Mandatory	–	–	-10	dB
18Mbps	Optional	–	–	-13	dB
24Mbps	Mandatory	–	–	-16	dB
36Mbps	Optional	–	–	-19	dB
48Mbps	Optional	–	–	-22	dB
54Mbps	Optional	–	–	-25	dB
Transmit modulation accuracy in 802.11n mode					
MCS7	As specified in IEEE 802.11n	–	–	-27	dB
Transmit modulation accuracy in 802.11ac mode					
MCS8	VHT20	–	–	-30	dB
MCS9	VHT20	–	–	-32	dB
Transmit power-on and power-down ramp time in 802.11b mode					
Transmit power-on ramp time from 10% to 90% output power		–	–	2	µs
Transmit power-down ramp time from 90% to 10% output power		–	–	2	µs
Other spectral parameters					
Spurious emissions at the antenna port	30MHz ~ 1GHz BW=100kHz	–	–	-62	dBm
	1GHz ~ 12.75GHz BW=1MHz	–	–	-47	dBm

BLUETOOTH RF SPECIFICATIONS

Table 44. Bluetooth RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
GFSK					
Output Power	Average Power	–	11	–	dBm
Frequency Range		2402	–	2480	MHz
Carrier Frequency Drift	DH1	-25	–	25	kHz
	DH3	-40	–	40	kHz
	DH5	-40	–	40	kHz
	Maximum Drift Rate	-20	–	20	kHz
Modulation	dF1 Avg	140	–	175	kHz
	dF2 Max	115	–	–	kHz
	dF1 Avg / dF2 Avg	80	–	–	%
Sensitivity (BER)	BER ≤0.1%	–	–	-70	dBm
Maximum Input Level	BER ≤0.1%	-20	–	–	dBm
EDR (DPSK)					
Relative Power	π/4-DQPSK	-4.0	–	1.0	dB
8DPSK		-4.0	–	–	dB
RMS DEVM	π/4-DQPSK	–	–	20.0	%
	8DPSK	–	–	13.0	%
Peak DEVM	π/4-DQPSK	–	–	35.0	%
	8DPSK	–	–	25.0	%
99% DEVM	π/4-DQPSK DEVM ≤ 0.30	99	–	–	%
	DEVM ≤ 0.20 8DPSK	99	–	–	%
EDR Sensitivity (BER)	π/4-DQPSK BER ≤ 0.01%	–	–	-70	dBm
	BER ≤ 0.01% 8DPSK	–	–	-70	dBm
EDR Maximum Input Level	π/4-DQPSK BER ≤ 0.1%	-20	–	–	dBm
	BER ≤ 0.1% 8 DPSK	-20	–	–	dBm
Low Energy					
Output Power	Output Power	-20	–	10	dBm
Operating Frequency	2402+K*2MHz (K=0~39)	2400	–	2483.5	MHz

ZigBee RF Receive Specifications

Receive measurements were collected with the ZigBee SoC Ceramic Balun Reference Design (Version A0) at 2440MHz. The typical number indicates one standard deviation above the mean, measured at room temperature (25°C). The Min and Max numbers were measured over process corners at room temperature.

Table 45. ZigBee RF Receive Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	–	2500	MHz
Sensitivity (boost mode)	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	–	-102	-96	dBm
Sensitivity	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	–	-100	-94	dBm
High-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	35	–	dB
Low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	35	–	dB
2nd high-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	46	–	dB
2nd low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	46	–	dB
High-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	39	–	dB
Low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	47	–	dB
2nd high-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	49	–	dB
2nd low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	49	–	dB
High-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	44	–	dB
Low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	47	–	dB
2nd high-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	59	–	dB
2nd low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	59	–	dB
Channel rejection for all other channels	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	40	–	dB
802.11g rejection centered at +12 MHz or -13 MHz	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	36	–	dB
Maximum input signal level for correct operation		0	–	–	dBm
Co-channel rejection	IEEE 802.15. 4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	-6	–	dBc
Relative frequency error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		-120	–	+120	ppm
Relative timing error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		-120	–	+120	ppm
Linear RSSI range	As defined by IEEE 802.15.4-2003	40	–	–	dB
RSSI Range		-90	–	-40	dB

ZigBee RF Transmit Specifications

Transmit measurements were collected with the Silicon Labs ZigBee SoC ceramic balun reference design (Version A0) at 2440 MHz. The typical number indicates one standard deviation below the mean, measured at room temperature of 25°C. The Min and Max numbers were measured over process corners at room temperature. In terms of impedance, this reference design presents a 3n3 inductor in parallel with a 100:50 balun to the RF pins.

Table 46. ZigBee Transmit Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power (boost mode)	At highest boost mode power setting (+8)	–	8	–	dBm
Maximum output power	At highest normal mode power setting (+3)	1	5	–	dBm
Minimum output power	At lowest power setting	–	-55	–	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	–	5	15	%
Carrier frequency error		-40	–	+40	ppm
PSD mask relative	3.5 MHz away	-20	–	–	dBm
PSD mask absolute	3.5 MHz away	-30	–	–	dBm

ARTIK 520 Module Mechanical Specifications

The ARTIK 520 Module supports three connectors and three RF connectors on a 25.0mmx30.0mm footprint. The size is 25.0mmx 37.0mm if the additional debug connector is included. Refer to section *ARTIK 520 Module Antenna Connections* for RF connector details. *Figure 11* shows the physical dimensions of the Top View, Bottom View and the Side View of the ARTIK 520 Module. All mechanical dimensions mentioned in this section are preliminary and could change.

Table 47. Connectors J3, J4, J5

	Connector Part Number	Number of pins	Pin pitch	Mating Part
Connector J3	Panasonic AXT460124	60	0.4mm	Panasonic AXT360124 (mated height 1.5mm) AXT360224 (mated height 2.5mm)
Connector J4				
Connector J5				

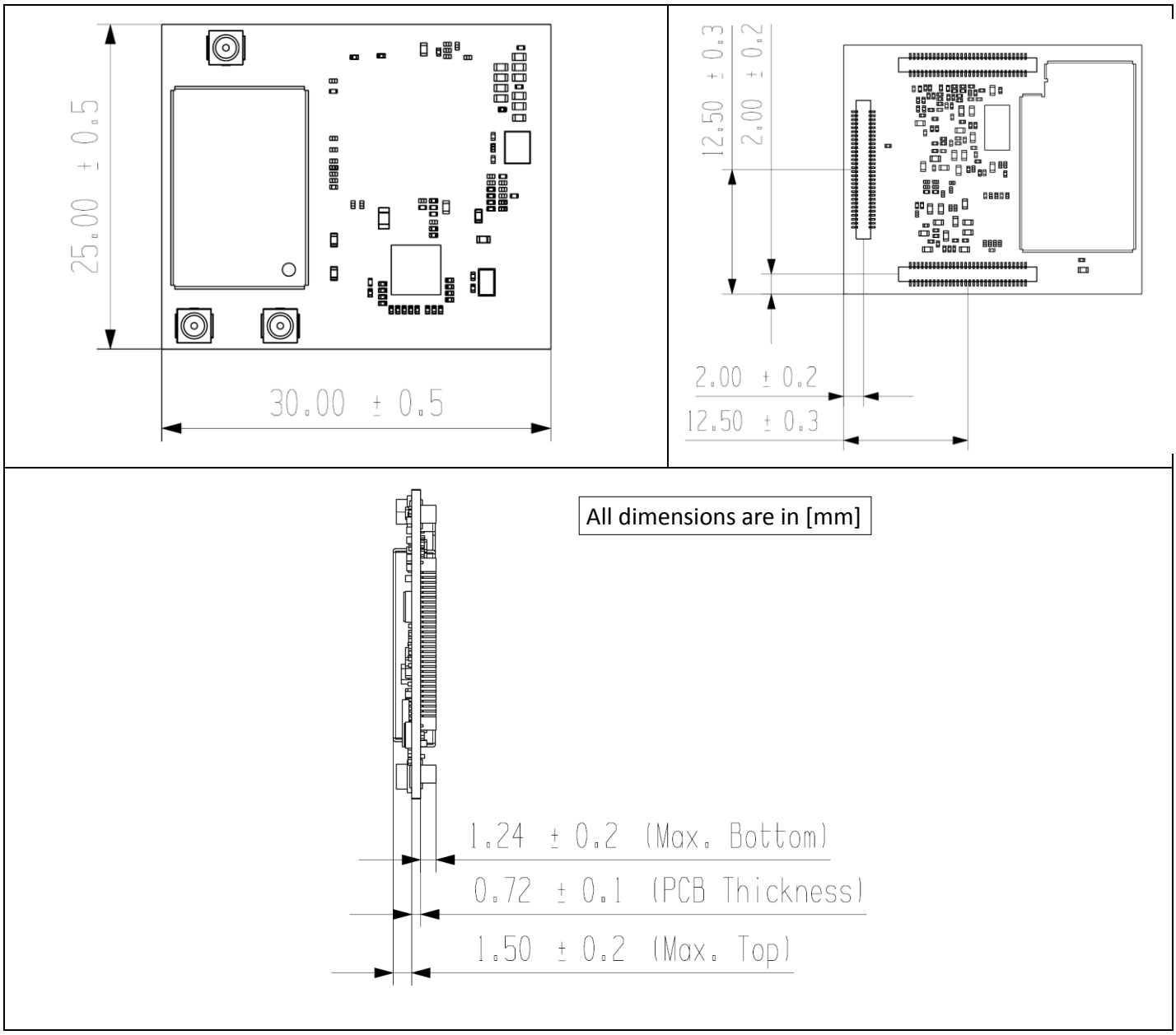

Figure 11. Mechanical Dimensions

Ordering Information

For volume ordering of the evaluation kits, please contact a sales representative in your area or email sales@artik.io.

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